IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC.,	)	
	)	
Plaintiff,	)	
	)	
v.	)	Civil Action No. 06-788 (JJF)
	)	
FREESCALE SEMICONDUCTOR, INC.,	)	
	)	**REDACTED**
Defendant.	)	**PUBLIC VERSION**

PLAINTIFF PROMOS TECHNOLOGIES, INC.'S
BRIEF IN ANSWER TO FREESCALE'S MOTION TO COMPEL

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CASES:

Plaintiff ProMOS Technologies, Inc. ("ProMOS") respectfully submits this brief in answer to the motion to compel filed by defendant Freescale Semiconductor, Inc. ("Freescale") on August 23, 2007, which appears to have been filed in the hope of blunting the force of the motion to compel filed by ProMOS earlier that same day. Freescale's motion is baseless and should be denied.

First, while seeking to compel supplemental infringement contentions for each and every accused Freescale product, Freescale has steadfastly refused to produce circuit diagrams or any other detailed technical documents showing the design or layout of the accused products. Freescale's failure to produce technical documents for its products is the principal subject of ProMOS's pending motion to compel, and as is made clear in that motion Freescale itself has made it impossible for ProMOS to provide more extensive and definitive infringement contentions.

Second, Freescale asks this Court to compel ProMOS to produce supplemental infringement contentions for the Fortin patent, notwithstanding that the parties already have in place an express agreement that ProMOS will do so by September 17, 2007. That Freescale has raised this issue with the Court makes clear that the instant motion is merely Freescale's way of getting before the Court discovery complaints – no matter how weak or unnecessary – in an effort to put a fig leaf over Freecale's own serious and massive failure to produce technical documents in this case.

Third, Freescale asks this Court to compel ProMOS to disclose certain licensing information even though ProMOS already has provided complete answers to the written discovery served by Freescale and does not have possession, custody or control over the license agreements Freescale is apparently seeking.

Finally, it should be noted that ProMOS has bent over backwards to obtain timely discovery from Freescale, which would have avoided many of the issues raised in Freescale's motion. The parties held telephone conferences relating to these issues on May 23, 2007, June 28, 2007, July 5, 2007, July 20, 2007, July 26, 2007, August 8, 2007, and August 17, 2007, and ProMOS wrote numerous letters to Freescale's counsel regarding these disputes. ProMOS also filed a motion to compel with the Court of July 6, 2007 asking that Freescale be required to produce basic technical documents. Based on representations made by Freescale regarding a timeline for production of such documents, ProMOS withdrew the motion to compel. But with the motion withdrawn, and the next non-dispositive motion deadline weeks away, Freescale failed to live up to its representations, and ProMOS was forced to seek emergency assistance from the Court and then to file another motion to compel. It is thus deeply ironic that, having painstakingly avoided complying with its own discovery obligations over the course of months, Freescale has moved the Court to compel ProMOS to produce infringement contentions based on technical information relating to the accused products which Freescale is continuing to withhold.

Because Freescale's motion lacks merit, the Court should deny it and award ProMOS its costs and expenses, including attorneys' fees, in responding to the motion.

PROCEDURAL BACKGROUND

On December 22, 2006, ProMOS filed this action against Freescale, a manufacturer of semiconductors, alleging infringement of three of ProMOS's patents: (i) U.S. Patent No. 5,488,709 entitled "Cache Including Decoupling Register Circuits" ("the '709 patent"), (ii) U.S. Patent No. 5,732,241 entitled "Random Access Cache Memory Controller and System" ("the '241 patent"), and (iii) U.S. Patent No. 6,670,267 entitled "Formation of Tungsten-Based Interconnect Using Thin Physically Vapor Deposited Titanium Nitride Layer" ("the '267 patent"). Both the

'709 patent and the '241 patent involve cache memory, a supplementary memory system that temporarily stores frequently-used instructions and data for quicker processing by the central processor of a computer. The '267 patent claims a method for manufacturing semiconductors using titanium nitride.

Although Freescale seeks to dismiss this action as a "revenge" lawsuit, it is well aware that the parties spent months before litigation discussing both ProMOS' and Freescale's patents and that any legal action by one party inevitably would be met by a counteraction from the other. Thus, it seems that Freescale merely resents the fact that ProMOS brought its patent infringement claims in this Court, in Delaware, where Freescale is incorporated, rather than following Freescale's lead of bringing those claims in the Eastern District of Texas. Freescale's disappointment that ProMOS selected Delaware as a forum over Freescale's preferred "home court" of Texas, however, does not provide any grounds for Freescale to insist upon adherence to Eastern District of Texas local rules or otherwise to have discovery in this case proceed as if it had been filed in Texas.

Freescale served its first set of interrogatories on ProMOS on April 11, 2007, and ProMOS answered those interrogatories on May 14, 2007. See Ex. A. In its answers, ProMOS provided Freescale with specific information regarding its infringement allegations, including a list of exemplary accused products, which ProMOS supplemented by letter on July 6, 2007. Ex. B. Attached to its interrogatory answers, ProMOS also provided Freescale with detailed documentation reading claim 1 of each of the Chan patents onto representative Freescale products and claim 47 of the Fortin patent onto a representative product. These materials – which are some 110-odd pages in length – identify, on an element-by-element basis, specific infringing aspects of the representative products and tie each element of the asserted claim to the specific part, process or function of the accused product. See Attachments to Ex. A. Moreover, ProMOS noted in its

interrogatory answers that "[f]ull identification of the asserted claims and identification of Freescale's infringement products and processes will be made through reports and testimony by ProMOS's experts in this action" and that "[a]dditional information in that regard is in the exclusive possession of Freescale. Accordingly, ProMOS reserves the right to supplement this response as discovery progresses." Ex. A (Answers to Interrogatories No. 1-3).

At the same time that Freescale served its interrogatories, ProMOS served Freescale with a set of document requests, a copy of which is attached hereto as Exhibit C. In relevant part, the requests sought basic technical documents necessary for ProMOS to present its infringement case at trial, including circuit diagrams (Request Nos. 46-49), drawings, schematics, and specifications (Request Nos. 27-30), reference and user manuals (Request No. 32), and manufacturing drawings (Request Nos. 33-37) of Freescale Products. As noted more fully in ProMOS's August 23, 2007 motion to compel, Freescale has refused to produce meaningful technical documents in response to these requests. Indeed, the vast majority of the materials produced by Freescale to date are comprised of the same publicly-available user manuals that are available on Freescale's website and that formed the basis for ProMOS's initial infringement contentions.

Critically absent from Freescale's production are any circuit diagrams or schematics of any of its cache memory systems that show the design or layout of the accused products in any amount of detail. Moreover, although Freescale has admitted that it maintains RTL documentation (a human-readable text format of circuit schematics which describes the structure of a circuit and the timing of interactions between elements with the circuit and that can be used to generate circuit diagrams), Freescale has refused to produce such materials pursuant to the normal protections of the Protective Order in this case. Instead, Freescale has taken the position that such materials will only be made available for review on a single off-line computer in the offices of their outside

counsel, Jones Day, and Freescale has refused to permit ProMOS's experts to make electronic copies of the RTL documentation so that they may run the appropriate software on the descriptions provided by the RTL documentation and generate the circuit diagrams. In light of Freescale's obstructionist conduct and the limited amount of design information presently available to ProMOS, it would make little sense for ProMOS to spend the time and money now to generate infringement charts reading each of the asserted claims onto each of the different accused products. Rather, as ProMOS repeatedly has suggested to Freescale, ProMOS should be permitted to supplement its infringement contentions, if necessary, by providing representative charts applying the independent claims of the Chan patents to representative product families after receiving and reviewing the circuit diagrams and detailed design information to which it is entitled.

ARGUMENT

I. FREESCALE'S REQUEST FOR AN ORDER COMPELLING PRODUCTION OF SUPPLEMENTAL INFRINGEMENT CONTENTIONS IS UNWARRANTED.

Freescale's primary complaint appears to be that, although Freescale was required to provide infringement contentions at the outset of its lawsuit against ProMOS in the Eastern District of Texas "before ProMOS had produced any documents," as required by the local rules of that Court, ProMOS has not followed the same course in this case. Freescale's Motion at 1. Freescale's frustration derives not from any misconduct on ProMOS's part, but rather from the unique attributes of the Local Patent Rules in the Eastern District of Texas, which impose obligations on plaintiffs in patent cases that go above and beyond the requirements imposed by the Federal Rules of Civil Procedure and the Local Rules of this Court. There simply is no basis – and Freescale has cited none – for requiring ProMOS to comply with Freescale's "contentions-first,

then discovery" mandate in a case before this Court, merely because Freescale prefers to litigate in the Eastern District of Texas. 1

In any event, the discovery record makes clear that Freescale alone is singularly responsible for the position in which it now finds itself. By obstinately refusing to produce circuit diagrams and/or permit ProMOS's experts to access Freescale's Computer Assisted Design ("CAD") databases for purposes of reviewing the same and generating circuit diagrams on their own, Freescale has succeeded in stonewalling meaningful discovery between the parties. Indeed, ProMOS has agreed to supplement its infringement contentions after Freescale provides ProMOS with either copies of circuit diagrams or access to the CAD databases – a sequence which is not only logical but also efficient. Nonetheless, Freescale has stuck tenaciously to the view that it should be permitted to skate through the discovery period without producing any meaningful design materials. As set forth more fully in ProMOS's pending motion to compel, it is Freescale, not ProMOS, which should be compelled to comply with its discovery obligations.

A. PROMOS SHOULD NOT BE REQUIRED TO SUPPLEMENT ITS RESPONSES TO CONTENTION INTERROGATORIES UNTIL FREESCALE PRODUCES TECHNICAL DOCUMENTS ON THE ACCUSED PRODUCTS, IN COMPLIANCE WITH FREESCALE'S OWN DISCOVERY OBLIGATIONS.

Freescale dismisses off-hand the 80-some pages of detailed infringement contentions relating to the Chan patents attached to ProMOS's interrogatory answers because the infringement

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1 While the Eastern District of Texas local patent rules may have some advantages, they also may produce disadvantages, in that they may require early infringement contentions that are less precise and that can result in wasted time and inefficiencies. Freescale's preliminary infringement contentions in its ED Texas case against ProMOS exemplify many of the shortcomings of documenting such contentions in advance of receiving discovery and definitive documentation on the accused products. Freescale's infringement contentions are replete with assumptions about ProMOS's products, some of which are inaccurate and may now require Freescale to backtrack on various steps taken in discovery. In any event, this Court, following the discovery rules applied in all federal court cases, generally allows for discovery of facts before requiring extensive responses to contention interrogatories.

contentions contained therein were "limited to two processor cores and one claim (claim 1) for each of the two patents." Freescale Motion at 6. Notably, Freescale has not argued that the infringement contentions are inadequate as they relate to the claims and products identified, but instead Freescale merely complains that ProMOS should have provided similar contentions applying each of the 26 claims (5 independent and 21 dependent) of the '709 patent and each of the 26 claims (4 independent and 22 dependent) of the '241 patent to each of 21 different processors. Freescale Motion at 7. 2/ In essence, Freescale is asking this Court to compel ProMOS to produce no fewer than 1,092 separate infringement charts (52 claims x 21 processors) – all before Freescale produces a single document reflecting in any amount of detail the design or layout of the Freescale products. Undertaking such a time-consuming task at this point would be a waste of time, because ProMOS ultimately will need to read the Chan patents onto more detailed circuit diagrams and schematics for Freescale's products.

Thus, the "pressing" problem of which Freescale complains, Freescale Motion at 7, is a problem of its own making. As set forth more fully in the August 23, 2007 motion to compel filed by ProMOS, Freescale has gone to great lengths to avoid producing documents showing the design or layout of the accused products in any amount of detail. Having done so, Freescale is hardly in a position to complain that ProMOS has failed to provide Freescale with detailed interrogatory answers applying each of the asserted claims to each of the accused products. Indeed, ProMOS

2/ Freescale also suggests that ProMOS's infringement contentions are less meaningful because they were created "before the litigation" and "given to Freescale in the course of licensing discussions relating to Freescale's patents." Freescale's Motion at 6. But as noted in ProMOS's motion to compel, Freescale's refusal to produce meaningful technical documents in discovery leaves ProMOS in the same position it was in before it filed suit – reliant for its infringement contentions upon publicly-available information such as user manuals contained on Freescale's website. Until Freescale produces the long-overdue circuit diagrams or permits ProMOS's experts to generate them on Freescale's computer system, ProMOS will have obtained no new information about the design or layout of the accused products through discovery.

has repeatedly informed Freescale that it is willing to supplement its interrogatory answers to read each of the independent claims of the patent onto representative products after Freescale produces design information relating to the accused products. See, e.g., Ex. A (Answers to Interrogatories No. 1-3). However, it would be both inefficient and unfair to force ProMOS to prepare such charts based on the limited materials that have been produced by Freescale to date – before Freescale produces a single document that shows in any amount of detail the design or layout of any of the accused products.

While Freescale is correct that the publicly-available materials produced by Freescale to date are sufficient to substantiate a claim of infringement, Freescale's Motion at 8-9, the publicly available user manuals are less precise and less detailed than the highly confidential design information reflected on circuit diagrams. It would be highly inefficient to force ProMOS to spend additional time and money supplementing its infringement contentions now, based purely on publicly available information, just to require ProMOS to turn around and produce additional charts that lay out ProMOS's infringement claims in more technical detail following Freescale's production of the long-overdue circuit diagrams or other equivalent detailed technical documentation. Instead, ProMOS should be permitted to supplement its infringement contentions with additional representative charts, to the extent necessary, following Freescale's production of meaningful design information, either in the form of circuit diagrams themselves or providing ProMOS's experts access to Freescale's computers for the purposes of generating such diagrams.

A similar approach has been taken by other courts in similar circumstances. See, e.g., Phillip M. Adams & Assocs., LLC v. Dell, Inc., Civil No. 1:05-CV-64, 2006 WL 2666408, *4 (D. Utah Sept. 15, 2006) (noting that a plaintiff in a district that requires preliminary infringement

contentions is required to provide defendant only with known information regarding infringement, and further noting that "[a]s discovery develops the entire field of allegedly infringing products, the claim charts will eventually be required to tell the entire story from Plaintiff's viewpoint."); Melvin v. United States, 14 Cl. Ct. 236, 238 (1988) ("Defendant's contentions that plaintiff is on a 'fishing expedition' aside, the Court is of the opinion that plaintiff is entitled to some discovery to support its broad claim that the F-16 infringes his patents. There is considerable merit to plaintiff's position that without the discovery he seeks, he is stymied from adequately supporting his claim because defendant controls exclusively the access to technical data that would assist plaintiff in specifying by name and claim the accused devices.").

The arguments made by Freescale in its motion do not compel a different result. To begin with, contrary to the suggestion implicit on page 9 of Freescale's motion, Freescale has not produced RTL documentation to ProMOS. Rather, Freescale has taken the position that it will only make the RTL documentation available for review on a single off-line laptop computer located in an isolated room in Jones Day's Cleveland office containing only the laptop, with no access to a printer and no opportunity to create electronic copies. As set forth more fully in ProMOS's motion to compel, Freescale's suggestion that the RTL documentation should be treated pursuant to Paragraph 4 of the Protective Order (relating to "computer code") – is way off base. As set forth more fully in the declaration attached to ProMOS's motion, RTL documentation is simply a human-readable format of design data, not a code that instructs a computer to perform functions. As a result, the highly-restrictive requirements of Paragraph 4 of the Protective Order simply do not apply.

Notwithstanding that ProMOS's counsel and experts have collectively spent three full days in Cleveland reviewing the materials in the past week, ProMOS has been unable to generate any useful information from that review for a number of independent reasons:

- First, ProMOS was denied the opportunity to make electronic copies (or even, for that matter, hard copy printouts) of the RTL documentation. As a result, ProMOS has been unable to use applicable software to generate circuit diagrams from the RTL documentation – rendering it of limited utility to ProMOS. Nor can ProMOS's experts even review the RTL documentation for two modules of the same product at the same time to see how they interact or compare.
- Second, the RTL materials were incomplete, comprising only a portion of the chip for many of the products, and completely lacking any information for other products.
- Third, the materials were produced in .txt format without any of the software that would normally be used by engineers to review, analyze, and convert the RTL documentation into schematics – thus rendering the materials of limited utility to ProMOS in terms of mapping the design of the products.

For all of the foregoing reasons, Freescale's production violates Rule 34 of the Rules of Civil Procedure, which requires Freescale to produce electronically stored information "as [it is] kept in the usual course of business" and "in a form or forms in which it is ordinarily maintained or in a form or forms that are reasonably usable." Rule 34(b)(i) and (ii). Moreover, Freescale's suggestion that ProMOS should be required to generate appropriately detailed infringement contentions by September 17, 2007 based on its limited review of incomplete RTL documentation to which it had severely limited access is untenable. Freescale Motion at 9.

Similarly, Freescale's assertion that ProMOS should be required to narrow its document requests to cover products that narrowly meet the elements of each of the Chan patents, Freescale Motion at 3-6, is unfounded. If Freescale had its way and ProMOS were required to propound requests narrowly relating to products that met each specific element of the Chan patent claims (whether such elements were spelled out or referenced as a whole), Freescale undeniably would take the position that none of its products met those elements and therefore that it was absolved from having to produce any responsive documents. Indeed, Freescale's counsel has made clear in past discussions that it is relying on a very contrived understanding of what a "port" is to come to the conclusion that Freescale's products that are located on a single chip by definition contain no ports. If Freescale were permitted to filter each document request through its own understanding of each of the claim terms, the discovery process would turn into a protracted fight about claim construction and the meaning of the claim terms. Moreover, ProMOS would have little or no ability to ascertain how Freescale's counsel was reading each of the claim terms (i.e., what is a port?) and applying them to the document-gathering process. Discovery would become a black box where Freescale's counsel had unilateral control over what it chose to produce and what it chose to withhold.

To avoid such problems and undue conflation of discovery and merits issues, the Federal Rules of Civil Procedure and this Court's local rules permit the parties broad latitude to conduct discovery without a need to prove the relevance or potential use of the information and documents sought before they are produced. Promos should be permitted to conduct discovery and receive meaningful responses from Freescale before it is required to supplement its infringement contentions. In particular, ProMOS is entitled to review the design information for each of Freescale's cache memory products and make its own determination about whether, for example,

each product has two ports as that term is construed by ProMOS. At least in that scenario, both parties are on equal footing when it comes to making arguments about whether a particular product does or does not meet the applicable claim limitations, and Freescale is not appointed final arbiter of any disputes about the meaning of claim terms.

Freescale also improperly suggests that ProMOS should be compelled to provide supplemental answers to Interrogatory No. 24, which sought ProMOS's claim construction contentions. As Freescale well knows, ProMOS proposed that the parties meet and confer to "establish a schedule pursuant to which the parties would simultaneously exchange proposed terms for construction, and then at a later date, proposed constructions for those terms, in advance of the date the parties' opening claim construction briefs are due." See Ex. D to Freescale's Motion. In a subsequent meet and confer, Freescale indicated that it would be willing to agree to such an approach, but stated that it would get back to ProMOS regarding appropriate dates for the exchanges. Rather than doing so, Freescale filed its motion to compel in violation of the meet and confer requirements of this Court. Its request therefore should be denied.

B. PROMOS HAS AGREED TO PROVIDE INFRINGEMENT CONTENTIONS FOR THE FORTIN PATENT BY SEPTEMBER 17, THEREBY MOOTING FREESCALE'S MOTION ON THIS ISSUE.

ProMOS is at a loss to understand why Freescale included this issue in its motion, other than to support a tit-for-tat rejoinder to the motion to compel that Freescale knew ProMOS intended to file seeking production of Freescale's long-overdue and promised technical documents. This issue is moot because, during the meet and confer process (after Freescale finally agreed to produce critical technical documents that would enable counsel for ProMOS to fully understand the relevant steps in the accused Freescale processes), ProMOS agreed that it would serve a supplemental response to Interrogatory No. 1 on September 17, 2007 setting forth more detailed

infringement contentions with respect to the Fortin patent. ProMOS does not anticipate that Freescale will have any basis for complaining about ProMOS's responses (other than that it might disagree with ProMOS's ultimate conclusions regarding infringement, which of course provides no grounds on which to file a motion to compel). However, even if Freescale did have such issues, it would be premature and contrary to the Local Rules for Freescale to attempt to raise those issues at the September 21 hearing.

In addition to improperly seeking relief on an issue that was mooted before the instant motion was filed, Freescale has attempted to support its motion with an incomplete and inaccurate version of the history of this dispute. The relevant facts are as follows: on July 10, 2007, counsel for ProMOS wrote to counsel for Freescale and requested additional process recipe and other information needed in order to fully understand the process flows Freescale had previously produced. Ex. D (July 10 e-mail from S. Jensen to K. Ferguson). Rather than producing the information to which ProMOS was entitled and had requested, Freescale instead took the position that none of the information ProMOS requested was relevant

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By letter dated August 10, Freescale shifted course and stopped pressing ProMOS for an answer to the hypothetical question posed in Interrogatory No. 18. See Ex. G. Instead, it agreed to the solution ProMOS had suggested in its August 7 letter. Specifically, Freescale agreed to produce the process recipe and other information it had been improperly withholding if ProMOS agreed to supplement its infringement contentions in response to Freescale's Interrogatory No. 1. In a subsequent meet and confer call, ProMOS agreed to do just that by September 17. 3/

Based on the sequence of events described above, it is entirely misleading for Freescale to suggest that ProMOS has been dragging its feet on this issue. ProMOS never refused to supplement its infringement contentions. It properly objected to the hypothetical question posed in Interrogatory No. 18 and took the logical and well-founded position that supplemental infringement contentions responsive to Interrogatory No. 1 should be required only after Freescale made a full and complete production of technical documents relating to the Fortin patent. If

3/ It should be noted that Freescale's initial production of process recipe and other technical information per the parties' agreement was incomplete. ProMOS requested supplemental information by email dated August 31. See Ex. H (e-mail from S. Jensen to M. Blackman). To date, Freescale has not promised to produce the requested information. Instead, it has responded only that it is looking into the issues raised by counsel for ProMOS's August 31 email. Ex. I (September 4 e-mail from M. Blackman to S. Jensen). ProMOS still intends to abide by its agreement to provide a supplemental contention interrogatory response on September 17. However, its ability to prepare that response is being hindered by Freescale's failure to make a full and complete production of the relevant technical documents.

Freescale had simply produced the process recipe and other information ProMOS requested months ago, rather than attempting to bargain for more detailed responses to interrogatories seeking ProMOS's contentions on hypothetical processes by withholding relevant discovery regarding Freescale's actual processes to which ProMOS was clearly entitled, Freescale would have received supplemental infringement contentions on the Fortin patent earlier than September 17.

Freescale's motion on this issue is also improper because it seeks responses to certain interrogatories that were not the subject of the parties' prior meet and confer conferences and/or are subject to different agreements. As set forth in Freescale's letter dated August 10, the parties agreed that ProMOS would supplement its infringement contentions responsive to Interrogatory No. 1 if Freescale produced critical process recipes and other technical information it had been withholding. However, in its motion, Freescale now seeks supplemental responses to Interrogatory Nos. 2, 3, 20 and 24 as well as Interrogatory No. 1. Interrogatories 2 and 3, which seek the basis for ProMOS's induced and contributory infringement contentions, were never part of the parties meet and confer discussions on this issue. Moreover, supplemental responses to these interrogatories should not be required because, as explained in ProMOS's initial responses to these interrogatories, ProMOS is only asserting a direct infringement claim with respect to the Fortin '267 process patent. See Ex. A to Freescale's Motion at 7, 10.

Interrogatories 20 and 24 seek ProMOS's claim construction contentions. In response to those interrogatories, ProMOS proposed that the parties meet and confer to "establish a schedule pursuant to which the parties would simultaneously exchange proposed terms for construction, and then at a later date, proposed constructions for those terms, in advance of the date the parties' opening claim construction briefs are due." See Ex. D to Freescale's Motion. In a subsequent

meet and confer, Freescale indicated that it would be willing to agree to such an approach, but stated that it would get back to ProMOS regarding appropriate dates for the exchanges. The supplemental interrogatory response ProMOS serves on September 17 will make clear how ProMOS construes the PVD claim terms as applied to Freescale's processes, but a discussion of any other claim construction issues in response to Interrogatory Nos. 20 and 24 is beyond the scope of the parties' agreement regarding the September 17 supplementation. Any such issues should instead be covered by the parties' agreement to meet and confer and establish dates for the simultaneous exchange of claim terms to be construed and proposed constructions for those terms.

Finally, although it is not at all relevant to the instant motion, Freescale is completely wrong in suggesting that "ProMOS has tried to obfuscate" the "differences between PVD and CVD [physical vapor deposition and chemical vapor deposition]." Freescale Br. at 11. To the contrary, as counsel for ProMOS has explained, developments in the art in recent years have blurred the distinction between chemical vapor deposition and physical vapor deposition, such that there is now overlap in the use and meaning of the terms. Such developments have been widely discussed in semiconductor literature, see, e.g., Ex. J, Handbook of Semiconductor Technology at 410 (noting that in so-called plasma-assisted chemical vapor deposition processes ("PACVD"), the ionized species being deposited are accelerated to the sample surface in response to the applied electromagnetic fields and that "the result is that the ion energy can be increased sufficiently to cause physical sputtering, or resputtering of the deposited films."), Ex. K, Laimer et al., "*Plasma-assisted chemical vapor deposition of titanium nitride in a capacitively coupled radio-frequency discharge*" at 2952, 2959 (describing PACVD as offering "a combination of advantages of both types of process [CVD and PVD]"), and Freescale is undoubtedly independently aware of these developments.

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As ProMOS has explained repeatedly to Freescale, any resolution of this issue must properly await expert analysis and possibly claim construction rulings, following an exchange of information about Freescale's products in discovery.

For the foregoing reasons, Freescale's motion to compel further interrogatory answers with respect to the Fortin patent should be denied.

II. FREESCALE'S COMPLAINTS ABOUT PROMOS'S ALLEGED FAILURE TO "PRODUCE LICENSING INFORMATION" ARE UNFOUNDED

Contrary to the suggestion in Freescale's Motion, ProMOS has provided complete and accurate responses to Freescale's discovery requests seeking information about any attempts to license the technology disclosed in the patents-in-suit.

See

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The fact that this issue might well become moot also counsels against the need for an *in limine* evidentiary ruling at this stage of the case. A ruling on this issue can and should be made, if necessary, closer to the trial date after all discovery has been completed and the parties have more thoroughly developed their damages cases for presentation to the jury.

CONCLUSION

For the foregoing reasons, Freescale's motion to compel should be denied.

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EXHIBIT A

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EXHIBIT B

FreeScale Processors

Product	Core
MPC5200	603e core
MPC5200B	603e core
	e200z1 core, optional
MPC5510	secondary e200z0 core
MPC5533	e200z3 core
MPC5534	e200z3 core
MPC5553	e200z6 core
MPC5554	e200z6 core
MPC5561	e200z6 core
MPC5565	e200z6 core
MPC5566	e200z6 core
MPC5567	e200z6 core
MPC7410	G4/e600 core
MPC7445	G4/e600 core
MPC7455	G4/e600 core
MPC7447	G4/e600 core
MPC7457	G4/e600 core
MPC7447A	G4/e600 core
MPC7448	G4/e600 core
MPC823	8xx core
MPC823E	8xx core
MPC850	8xx core
MPC852T	8xx core
MPC853T	8xx core
MPC855T	8xx core
MPC857DSL	8xx core
MPC857T	8xx core

MPC859DSL	8xx core
MPC859T	8xx core
MPC860	8xx core
MPC860P	8xx core
MPC862	8xx core
MPC866	8xx core
MPC870	8xx core
MPC875	8xx core
MPC880	8xx core
MPC885	8xx core
MPC8247	603e core
MPC8248	603e core
MPC8250	G2 core (603e der.)
MPC8255	G2 core (603e der.)
MPC8260	G2 core (603e der.)
MPC8264	G2 core (603e der.)
MPC8265	G2 core (603e der.)
MPC8266	G2 core (603e der.)
MPC8270	603e core
MPC8271	603e core
MPC8272	603e core
MPC8275	603e core
MPC8280	603e core
MPC8313	e300 core
MPC8313E	e300 core
MPC8321	e300c2 core
MPC8321E	e300c2 core
MPC8323	e300c2 core
MPC8323E	e300c2 core
MPC8343E	e300 core
MPC8347E	e300 core
MPC8349E	e300 core
MPC8358E	e300 core
MPC8360E	e300 core
MPC8533E	e500 v2 core
MPC8540	e500 core
MPC8541E	e500 core

MPC8543E	e500 core
MPC8544E	e500 core
MPC8545E	e500 core
MPC8547E	e500 core
MPC8548E	e500 core
MPC8555E	e500 core
MPC8560	e500 core
MPC8567E	e500 core
MPC8568E	e500 core
MPC8641	e600 core
MPC8641D	Dual e600 core
MCF5206e	ColdFire V2
MCF5207	ColdFire V2
MCF5208	ColdFire V2
MCF5211	ColdFire V2
MCF5212	ColdFire V2
MCF5213	ColdFire V2
MCF5214	ColdFire V2
MCF5216	ColdFire V2
MCF5232	ColdFire V2
MCF5233	ColdFire V2
MCF5234	ColdFire V2
MCF5235	ColdFire V2
MCF5249	ColdFire V2
MCF5270	ColdFire V2
MCF5271	ColdFire V2
MCF5272	ColdFire V2
MCF5274	ColdFire V2
MCF5274L	ColdFire V2
MCF5275	ColdFire V2
MCF5275L	ColdFire V2
MCF5280	ColdFire V2
MCF5281	ColdFire V2
MCF5282	ColdFire V2
MCF5307	ColdFire V3

MCF5327	ColdFire V3
MCF5328	ColdFire V3
MCF5329	ColdFire V3
MCF5372	ColdFire V3
MCF5372L	ColdFire V3
MCF5373	ColdFire V3
MCF5373L	ColdFire V3
MCF5407	ColdFire V4
MCF5470	ColdFire V4e
MCF5471	ColdFire V4e
MCF5472	ColdFire V4e
MCF5473	ColdFire V4e
MCF5474	ColdFire V4e
MCF5475	ColdFire V4e
MCF5480	ColdFire V4e
MCF5481	ColdFire V4e
MCF5482	ColdFire V4e
MCF5483	ColdFire V4e
MCF5484	ColdFire V4e
MCF5485	ColdFire V4e
MC68060	MC68060
MC68LC060	MC68060
MC68EC060	MC68060
i.MX1 (MC9328MX1)	ARM920T core
i.MX21	ARM926EJ-S core
i.MX21S	ARM926EJ-S core
i.MX27	ARM926EJ-S core
i.MX31	ARM1136JF-S core
i.MX31L	ARM1136JF-S core
i.MXL	ARM920T core
i.MXS	ARM920T core
MSC8144	Four 800 MHz/1 GHz StarCore SC3400 DSP extended cores
MSC8144E	Four 800 MHz/1GHz StarCore SC3400 DSP core subsystems

MSC8144EC	Four 800 MHz/1GHz StarCore SC3400 DSP core subsystems
MSC7110	SC1400 core
MSC7112	SC1400 core
MSC7113	SC1400 core
MSC7115	SC1400 core
MSC7116	SC1400 core
MSC7118	SC1400 core
MSC7119	SC1400 core
MSC7120	e300 core
DSP56301	DSP56300 core
DSP56311	DSP56300 core
DSP56321	DSP56300 core
DSP56L307	DSP56300 core

Description
16 KB instruction cache / 16 KB data cache
16 KB instruction cache / 16 KB data cache

L1: 1MB or 512 KB embedded flash; plus memory management unit with buffer
L1: 48KB cache; 768KB embedded flash; plus memory management unit with buffer
L1: 64KB cache; 1MB embedded flash; plus memory management unit with buffer

L1 (U-Cache): 8KB; L2: 64KB cache; 1.5MB embedded flash; plus memory management unit with buffer

L1 (U-Cache): 32KB; L2: 64KB cache; 2MB embedded flash; plus memory management unit with buffer

L1 (U-Cache): 32KB; L2: 192KB cache; 1MB embedded flash; plus memory management unit with buffer
L1 (U-Cache): 8KB; L2: 64KB cache; 2MB embedded flash; plus memory management unit with buffer

L1 (U-Cache): 32KB; L2: 128KB cache; 3MB embedded flash; plus memory management unit with buffer
L1 (U-Cache): 8KB; L2: 64KB cache; 2MB embedded flash; plus memory management unit with buffer
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB to 1 MB
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB to 1 MB
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB to 1 MB
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB to 1 MB
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB to 1 MB
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB to 1 MB
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB to 1 MB
2 KB instruction cache / 1 KB data cache
16 KB instruction cache / 8 KB data cache
2 KB instruction cache / 1 KB data cache
4 KB instruction cache / 4 KB data cache
4 KB instruction cache / 4 KB data cache
4 KB instruction cache / 4 KB data cache
4 KB instruction cache / 4 KB data cache
4 KB instruction cache / 4 KB data cache

16 KB instruction cache / 8 KB data cache
16 KB instruction cache / 8 KB data cache
4 KB instruction cache / 4 KB data cache
16 KB instruction cache / 8 KB data cache
16 KB instruction cache / 8 KB data cache
16 KB instruction cache / 8 KB data cache
8 KB instruction cache / 8 KB data cache
8 KB instruction cache / 8 KB data cache
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16 KB instruction cache / 16 KB data cache
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32 KB instruction cache / 32 KB data cache
32 KB instruction cache / 32 KB data cache
32 KB instruction cache / 32 KB data cache
32 KB instruction cache / 32 KB data cache
32 KB instruction cache / 32 KB data cache
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB

32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB
32 KB instruction cache / 32 KB data cache; L2 cache: 512 KB
32 KB instruction cache / 32 KB data cache; L2 cache: 512 KB
32 KB instruction cache / 32 KB data cache; L2 cache: 512 KB
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB
32 KB instruction cache / 32 KB data cache; L2 cache: 256 KB
32 KB instruction cache / 32 KB data cache; L2 cache: 512 KB
32 KB instruction cache / 32 KB data cache; L2 cache: 512 KB

1 MB L2 cache; 32 KB instruction cache / 32 KB data cache; Dual 64-bit DDR and DDR2 memory controllers
1 MB L2 cache per core; 32 KB instruction cache / 32 KB data cache; Dual 64-bit DDR and DDR2 memory controllers
4KB I-Cache; 8 KB SRAM
8KB I/D-Cache; 16KB SRAM
8KB I/D-Cache; 16KB SRAM
16KB SRAM; 128 KB Embedded Flash memory (No cache?)
32KB SRAM; 256 KB Embedded Flash memory (No cache?)
32KB SRAM; 256 KB Embedded Flash memory (No cache?)
2KB I-Cache; 64KB SRAM; 256 KB Embedded Flash memory
2KB I-Cache; 64KB SRAM; 512 KB Embedded Flash memory
8KB configurable I/D-Cache; 64KB SRAM
8KB configurable I/D-Cache; 64KB SRAM
8KB configurable I/D-Cache; 64KB SRAM
8KB configurable I/D-Cache; 64KB SRAM
8KB I/D-Cache; 96KB SRAM
8KB configurable Cache; 64KB SRAM
8KB configurable Cache; 64KB SRAM
1KB I-Cache; 4KB SRAM
16KB configurable Cache; 64KB SRAM
16KB configurable Cache; 64KB SRAM
16KB configurable Cache; 64KB SRAM
16KB configurable Cache; 64KB SRAM
2KB I-Cache; 64KB SRAM
2KB I-Cache; 64KB SRAM; 256 KB Embedded Flash memory
2KB I-Cache; 64KB SRAM; 512 KB Embedded Flash memory
8KB unified Cache; 4KB SRAM

16KB I/D-Cache; 32KB SRAM
16KB I/D-Cache; 32KB SRAM
16KB I/D-Cache; 32KB SRAM
16KB I/D-Cache; 32KB SRAM
16KB I/D-Cache; 32KB SRAM
16KB I/D-Cache; 32KB SRAM
16KB I/D-Cache; 32KB SRAM
16KB I-Cache; 8KB D-Cache; 4KB SRAM
32KB I-Cache; 32KB D-Cache; 32KB SRAM
32KB I-Cache; 32KB D-Cache; 32KB SRAM
32KB I-Cache; 32KB D-Cache; 32KB SRAM
32KB I-Cache; 32KB D-Cache; 32KB SRAM
32KB I-Cache; 32KB D-Cache; 32KB SRAM
32KB I-Cache; 32KB D-Cache; 32KB SRAM
32KB I-Cache; 32KB D-Cache; 32KB SRAM
32KB I-Cache; 32KB D-Cache; 32KB SRAM
32KB I-Cache; 32KB D-Cache; 32KB SRAM
32KB I-Cache; 32KB D-Cache; 32KB SRAM
32KB I-Cache; 32KB D-Cache; 32KB SRAM
Dual 8KB on-chip Caches
Dual 8KB on-chip Caches
Dual 8KB on-chip Caches
16KB instruction Cache, 16KB data Cache
16KB instruction Cache, 16KB data Cache
16KB instruction Cache, 16KB data Cache
16KB instruction Cache, 16KB data Cache
16KB instruction Cache, 16KB data Cache; L2: 128 KB unified Cache
16KB instruction Cache, 16KB data Cache; L2: 128 KB unified Cache
16KB instruction Cache, 16KB data Cache
16KB instruction Cache, 16KB data Cache
Four 16-Kbyte L1 instruction cache (one per core); Four 32-Kbyte L1 data cache (one per core); One 128-Kbyte shared L2 instruction cache; One 512-Kbyte shared M2 memory for critical data and temporary data buffering; 10 Mbytes of 128-bit wide shared M3 memory
Four 16-Kbyte L1 instruction cache (one per core); Four 32-Kbyte L1 data cache (one per core); One 128-Kbyte shared L2 instruction cache; One 512-Kbyte shared M2 memory for critical data and temporary data buffering; 10 Mbytes of 128-bit wide shared M3 memory

Four 16-Kbyte L1 instruction cache (one per core); Four 32-Kbyte L1 data cache (one per core); One 128-Kbyte shared L2 instruction cache; One 512-Kbyte shared M2 memory for critical data and temporary data buffering; 10 Mbytes of 128-bit wide shared M3 memory

64 KB of SRAM memory, a 16 KB 16-way Instruction Cache

192 KB of SRAM memory, a 16 KB 16-way Instruction Cache

192 KB of SRAM memory, a 16 KB 16-way Instruction Cache

384 KB of SRAM memory, a 16 KB 16-way Instruction Cache

384 KB of SRAM memory, a 16 KB 16-way Instruction Cache

448 KB of SRAM memory, a 16 KB 16-way Instruction Cache

448 KB of SRAM memory, a 16 KB 16-way Instruction Cache

16 KB instruction cache and a 16 KB data cache

1024-4096 x 24-bit Program RAM (optional configurations)with 1024 x 24-bit Instruction Cache (if enabled); 2048/3072 x 24-bit X data RAM (optional configuration); 2048/3072 x 24-bit Y data RAM (optional configuration)

128 K x 24-bit on-chip RAM total; Program RAM, instruction cache, X data RAM, and Y data RAM sizes are variable

192 K x 24-bit on-chip RAM total; Program RAM, instruction cache, X data RAM, and Y data RAM sizes are variable

64 K x 24 on-chip RAM total; Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable; 192 x 24-bit bootstrap ROM

EXHIBIT C

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC.,	)	
	)	
Plaintiff,	)	C.A. No. 06-788-JJF
	)	
v.	)	
	)	
FREESCALE SEMICONDUCTOR, INC.,	)	
	)	
Defendant.	)	

PLAINTIFF PROMOS TECHNOLOGIES, INC.'S
FIRST SET OF REQUESTS FOR PRODUCTION OF DOCUMENTS AND THINGS
FROM DEFENDANT FREESCALE SEMICONDUCTOR, INC. (Nos. 1-117)

Pursuant to Rules 34 and 26 of the Federal Rules of Civil Procedure, Plaintiff ProMOS Technologies, Inc. ("ProMOS") hereby requests that defendant Freescale Semiconductor, Inc. ("Freescale") produce for inspection and/or copying the following documents and things at the offices of Hogan & Hartson, LLP, Columbia Square, 555 13th Street, N.W., Washington, D.C., 20004, or such other mutually agreed upon location, within thirty (30) days of the date of service of these requests.

DEFINITIONS

1. The terms "Plaintiff" and "ProMOS" refer to ProMOS Technologies, Inc., and its officers, agents, employees, and representatives.

2. The terms "Defendant," "you," "your," and "Freescale" refer to Defendant Freescale Semiconductor, Inc., including but not limited to its divisions, subsidiaries, directors, agents, representatives, attorneys and employees, and any predecessor in interest.

3. The term "Complaint" means the Complaint and any amended Complaints filed by Plaintiff in this action.

4. The term "Answer" means the Answer and Affirmative Defenses, or any amendments thereto, filed by Defendant in this action. Whenever a request refers to or quotes from the Answer, all words in the request have the same meaning as in the Answer.

5. The term "Counterclaims" means the Counterclaims, or any amendments thereto, filed by Defendant in this action. Whenever a request refers to or quotes from the Counterclaims, all words in the request have the same meaning as in the Counterclaims.

6. The term "document" as used herein is employed in the broadest possible sense under Rule 34 and includes, but is not limited to, any printed, written, recorded, taped, electronic (including e-mail and deleted electronic media that is recoverable in any form), graphic, or other tangible matter from whatever source, however produced or reproduced, whether in draft or otherwise, whether sent or received or neither, including the original, all amendments and addenda and any non-identical copy (whether different from the original because of notes made on or attached to such copy or otherwise) of any and all writings, correspondence, letters, telegraphs, telex communicants, cables, notes, notations, papers, newsletters, memoranda, interoffice communications, e-mails, releases, agreements, contracts, books, pamphlets, studies, minutes of meetings, recordings or other memorials of any type of personal or telephone conversations, meetings or conferences, reports, analyses, test results, examinations, evaluations, estimates, projections, forecasts, receipts, statements, accounts, books of account, diaries, calendars, desk pads, appointment books, stenographer's notebooks, transcripts, ledgers, registers, worksheets, journals, statistical records, cost sheets, summaries, lists, tabulations, digests, canceled or uncanceled checks or drafts, vouchers, charge slips, invoices, purchase orders, hotel charges, accountant's reports, financial statements, newspapers, periodicals or magazine materials, and any materials underlying, supporting, or used in the preparation of any

documents. The term "document(s)" also specifically includes any records stored on computer tape or computer disk or otherwise stored by or in a computer, including telephone voice mail or electronic mail, whether or not a hard copy (i.e., paper copy) of the document is or was at any time in existence. A document includes all documents appended thereto. The documents requested shall include all marked copies. A "marked copy" is any document containing any writing or any markings of any kind in the text, in the margins, or on the reverse side of the document.

7. The term "person(s)" includes any natural person, corporation, partnership, association, joint venture, sole proprietorship, firm, business enterprise, governmental or quasi-governmental body or agency, or legal entity of any type, and includes both the singular and plural.

8. The term "communications" means all oral, visual, or other sensory means of transmitting information, messages, or statements, including but not limited to correspondence, letters, memoranda, e-mails (with any attachment(s)), meeting minutes, transcripts of telephone conversations, and presentations.

9. The terms or phrases "relating to," "relate(s)," or "related to" includes, but is not limited to, constituting, comprising, consisting of, containing, setting forth, describing, discussing, citing, regarding, pertaining to, mentioning, proposing, showing, disclosing, containing, analyzing, explaining, summarizing, supporting, evidencing, authorizing, concerning, embodying, reflecting, identifying, incorporating, considering, recommending, continuing, enumerating, dealing with, commenting on, referring to directly or indirectly, dealing with, responding to, or in any way logically or factually relevant to the matter described in the request.

10. The term "date" means the exact day, month and year, if ascertainable, or, if not, the best available approximation, including relationship to other events.

11. The terms "and" as well as "or" shall be construed either disjunctively or conjunctively as necessary to bring within the scope of these requests any documents that otherwise would be construed to be outside their scope.

12. The terms "ProMOS patents," "ProMOS patents-in-suit," and "patents-in-suit," mean United States Letters Patent No. 5,488,709 ("the '709 patent") entitled "Cache Including Decoupling Register Circuits;" United States Letters Patent No. 5,732,241 ("the '241 patent") entitled "Random Access Cache Memory Controller and System;" and United States Letters Patent No. 6,670,267 ("the '267 patent") entitled "Formation of Tungsten-Based Interconnect Using Thin Physically Vapor Deposited Titanium Nitride Layer."

13. With respect to the '709 patent and the '241 patent, the term "inventor" shall mean Alfred K. Chan. With respect to the '267 patent, the term "inventor" shall mean Vincent Fortin. The term "inventors" shall mean Messrs. Chan and Fortin together.

14. The term "infringement" shall be defined broadly to include direct, contributory and induced infringement under the applicable laws.

15. The term "market," as a verb, shall mean to sell, lease, license, exhibit or distribute; or to offer to sell, lease, license, exhibit or distribute.

16. The term "sale" means and refers to any exchange of goods, services or other property for value and includes transferring goods to another party on a consignment basis, regardless of whether title has passed.

17. As used herein, "prior art" includes any reference or subject matter set forth in or relevant under 35 U.S.C. § 102 and 35 U.S.C. § 103.

18. The term "Freescale Product(s)" includes: microcontrollers, microprocessors, processors, digital signal processors, controller cores, processor cores and all other components or goods you manufacture or market for sale or sell in any way that use, incorporate, work with or rely on cache memory; systems, components, products and goods that use, incorporate work with or rely on microcontrollers, microprocessors, processors, digital signal processors, controller cores, processor cores or other components or goods that use, incorporate, work with or rely on cache memory; and integrated circuits and semiconductor products that incorporate one or more conductors that includes a layer of tungsten overlying a layer of titanium nitride, such conductors including, but not limited to, those formed using Damascene and dual Damascene processes.

INSTRUCTIONS

1. In responding to these requests, you shall furnish all documents that are in your possession, custody, or control; or are within the possession, custody, or control of your officers, directors, employees, agents, representatives, present or former contractors, consultants, investigators, or attorneys; or otherwise available to you, regardless of whether documents are possessed directly by you, or any parent, subsidiary or affiliated corporation, or any of such entity's officers, directors, employees, agents, representatives, present or former contractors, consultants, investigators or attorneys.

2. Organize and label each document or set of documents, indicating by number the request to which the document(s) relates. In your written response, provide the document production (i.e. "Bates") number(s) for document(s) responsive to each request.

3. Electronic and computerized information must be produced in an intelligible format or together with a description of the system from which it was derived sufficient to permit rendering of the materials intelligible.

4. If any document responding to all or any part of this Request is not currently available, include a statement to that effect and furnish whatever documents are available. Include in your statement when such documents were most recently in your possession or subject to your control and what disposition was made of them, identifying the name, job title, and the last known address of each person currently in possession or control of such documents. If any of such documents were destroyed, identify the name, job title and the last known business address of each person who directed that the documents be destroyed, and state the reasons the documents were destroyed. If you do not have a document responsive to a request, but you know of person(s) or organization(s) who may have all or any portion of the document, then all such information, including names, addresses, and telephone numbers, shall be disclosed in your written response.

5. If any document or portion of any document covered by this Request for Production is withheld from production due to a claim of privilege, protection, or other grounds for non-disclosure, furnish a list of all such documents withheld that provides the following information: (a) the "Bates" number(s); (b) the identity of the person(s) who prepared or authorized the preparation of the document and, if applicable, the person(s), addresses, and organization to whom the document was sent or shown; (c) the date (or your best approximation thereof) on which the document was prepared; (d) a description of the type of document (e.g., letter, ledger, etc.); (e) the subject matter of the document; (f) a brief reason why the document is claimed to be privileged, protected, or subject to non-disclosure; and (g) the paragraph(s) of this Request to which the document responds.

6. This Request is continuing and requires, to the extent authorized by Rule 26(e) of the Federal Rules of Civil Procedure, production of any additional responsive documents that

may be located or acquired by you or your employees after the date of your original production.

7. Unless otherwise indicated in a particular request, the relevant time period for each Request shall be from January 1, 2000, to the present.

SPECIFIC REQUESTS FOR PRODUCTION

REQUEST NO. 1:

All documents identified, requested to be identified, relied upon, reviewed, or consulted in responding to Plaintiff's First Set of Interrogatories to Defendant.

REQUEST NO. 2:

All written policies, procedures and guidelines related to Freescale's computers, computer systems, electronic data and electronic media that hold, contain, save, or manage documents, including, but not limited to, (a) back up tape rotation schedules; (b) electronic data retention, preservation and destruction schedules; (c) employee use of company computers and data; (d) file naming conventions and standards; (e) diskette, CD, DVD, and other removable media labeling standards; and (e) e-mail storage (i.e., limitations on mailbox sizes and storage locations).

REQUEST NO. 3:

Documents sufficient to show your document retention and/or destruction policies and/or practices from 2000 to the present.

REQUEST NO. 4:

Organizational charts for all of your Information Technology-related or Information Services-related departments or divisions.

REQUEST NO. 5:

Documents sufficient to show your past and present organizational and operational structure, including all divisions or subsidiaries, entities owned or controlled by

Freescale, affiliates, predecessors or successors in interest, whether in the United States, or anywhere else in the world, and the identity of the officers and managers of each such entity.

REQUEST NO. 6:

All documents that identify present employees, past employees, consultants, and contract employees, whether full or part time, whose responsibilities or assignment include work relating to the conception, design, development, manufacture, analysis, testing, marketing, sales or repair of each Freescale Product, including but not limited to, organizational charts and telephone or email directories.

REQUEST NO. 7:

All documents that identify present employees, past employees, consultants, and contract employees, whether full or part time, whose responsibilities or assignment include work relating to the conception, design, development, manufacture, analysis, testing, marketing, sales or repair of each cache memory used with or in, incorporated in or relied on by a Freescale Product, including but not limited to, organizational charts and telephone or email directories.

REQUEST NO. 8:

All documents that identify present employees, past employees, consultants, and contract employees, whether full or part time, whose responsibilities or assignment include work relating to the conception, design, development, manufacture, analysis, testing, marketing, sales or repair of any register(s) used in writing, reading, buffering or accessing data from or to each cache memory used with or in, incorporated in or relied on by a Freescale Product, including but not limited to, organizational charts and telephone or email directories.

REQUEST NO. 9:

All documents that identify present employees, past employees, consultants, and

contract employees, whether full or part time, whose responsibilities or assignment include work relating to the conception, design, development, manufacture, analysis, testing, marketing, sales or repair of each cache controller used with or in, incorporated in or relied on by a Freescale Product, including but not limited to, organizational charts and telephone or email directories.

REQUEST NO. 10:

All documents that identify present employees, past employees, consultants, and contract employees, whether full or part time, whose responsibilities or assignment include work relating to the conception, design, development, manufacture, analysis, testing, marketing, sales or repair of each process for forming conductors that include a layer of tungsten overlying a layer of titanium nitride used with or in, incorporated in or relied on by a Freescale Product, including but not limited to, organizational charts and telephone or email directories.

REQUEST NO. 11:

Documents sufficient to identify, describe, illustrate, or depict names and/or functions of subsidiaries, departments, or divisions that were involved in any manner in the conception, design, development, manufacture, analysis, testing, marketing, sales or repair of any Freescale Product.

REQUEST NO. 12:

Documents sufficient to identify, describe, illustrate, or depict names and/or functions of subsidiaries, departments, or divisions that were involved in any manner in the conception, design, development, manufacture, analysis, testing, marketing, sales or repair of each cache memory used with, incorporated in or relied on by any Freescale Product.

REQUEST NO. 13:

Documents sufficient to identify, describe, illustrate, or depict names and/or

functions of subsidiaries, departments, or divisions that were involved in any manner in the conception, design, development, manufacture, analysis, testing, marketing, sales or repair of any register(s) used in writing, reading, buffering or accessing data from or to each cache memory used with or in, incorporated in or relied on by a Freescale Product.

REQUEST NO. 14:

Documents sufficient to identify, describe, illustrate, or depict names and/or functions of subsidiaries, departments, or divisions that were involved in any manner in the conception, design, development, manufacture, analysis, testing, marketing, sales or repair of each cache controller used with or in, incorporated in or relied on by a Freescale Product.

REQUEST NO. 15:

Documents sufficient to identify, describe, illustrate, or depict names and/or functions of subsidiaries, departments, or divisions that were involved in any manner in the conception, design, development, manufacture, analysis, testing, marketing, sales or repair of each process for forming conductors that include a layer of tungsten overlying a layer of titanium nitride used with or in, incorporated in or relied on by a Freescale Product.

REQUEST NO. 16:

All documents relating to third parties contracted, consulted, hired and/or retained that worked with Freescale or worked with another third party on Freescale's behalf on the conception, design, development, implementation, testing and manufacturing of each version of each model of Freescale Product, including but not limited to, contracts, contract proposals, Requests for Proposals (RFPs), solicitations, queries, investigations, and capability studies.

REQUEST NO. 17:

All documents relating to third parties contracted, consulted, hired and/or retained

that worked with Freescale or worked with another third party on Freescale's behalf on the conception, design, development, implementation, testing and manufacturing of each version of each cache memory used with, incorporated in or relied on by any Freescale Product, including but not limited to, contracts, contract proposals, Requests for Proposals (RFPs), solicitations, queries, investigations, and capability studies.

REQUEST NO. 18:

All documents relating to third parties contracted, consulted, hired and/or retained that worked with Freescale or worked with another third party on Freescale's behalf on the conception, design, development, implementation, testing and manufacturing of each version of each register(s) used in writing, reading, buffering or accessing data from or to each cache memory used with, incorporated in or relied on by a Freescale Product, including but not limited to, contracts, contract proposals, Requests for Proposals (RFPs), solicitations, queries, investigations, and capability studies.

REQUEST NO. 19:

All documents relating to third parties contracted, consulted, hired and/or retained that worked with Freescale or worked with another third party on Freescale's behalf on the conception, design, development, implementation, testing and manufacturing of each version of each cache controller used with, incorporated in or relied on by a Freescale Product, including but not limited to, contracts, contract proposals, Requests for Proposals (RFPs), solicitations, queries, investigations, and capability studies.

REQUEST NO. 20:

All documents relating to third parties contracted, consulted, hired and/or retained that worked with Freescale or worked with another third party on Freescale's behalf on the

conception, design, development, implementation, testing and manufacturing of each version of each process for forming conductors that include a layer of tungsten overlying a layer of titanium nitride used with or in, incorporated in or relied on by a Freescale Product, including but not limited to, contracts, contract proposals, Requests for Proposals (RFPs), solicitations, queries, investigations, and capability studies.

REQUEST NO. 21:

Your annual reports, prospectuses, proxy statements and Form 10-K and Form 10-Q reports for the years 2000 to the present.

REQUEST NO. 22:

All documents relating to design reviews and design review meetings, including but not limited to, all notes, minutes, reports, action item lists and management summaries, relating to each version of each model of Freescale Product.

REQUEST NO. 23:

All documents relating to design reviews and design review meetings, including but not limited to, all notes, minutes, reports, action item lists and management summaries, relating to each version of each cache memory used with, incorporated in or relied on by any Freescale Product.

REQUEST NO. 24:

All documents relating to design reviews and design review meetings, including but not limited to, all notes, minutes, reports, action item lists and management summaries, relating to each version of each register(s) used in writing, reading, buffering or accessing data from or to each cache memory used with, incorporated in or relied on by a Freescale Product.

REQUEST NO. 25:

All documents relating to design reviews and design review meetings, including but not limited to, all notes, minutes, reports, action item lists and management summaries, relating to each version of each cache controller used with, incorporated in or relied on by a Freescale Product.

REQUEST NO. 26:

All documents relating to design reviews and design review meetings, including but not limited to, all notes, minutes, reports, action item lists and management summaries, relating to each version of each process for forming conductors that include a layer of tungsten overlying a layer of titanium nitride used with or in, incorporated in or relied on by a Freescale Product.

REQUEST NO. 27:

All documents relating to drawings, schematics, blueprints, manufacturing specifications, engineering specifications, design specifications, product test specifications, part specifications, assembly specifications and other documents relating to the design, development, or manufacture of any Freescale Product.

REQUEST NO. 28:

All documents relating to drawings, schematics, blueprints, manufacturing specifications, engineering specifications, design specifications, product test specifications, part specifications, assembly specifications and other documents relating to the design, development, or manufacture of each cache memory used with, incorporated in or relied on by any Freescale Product.

REQUEST NO. 29:

All documents relating to drawings, schematics, blueprints, manufacturing specifications, engineering specifications, design specifications, product test specifications, part specifications, assembly specifications and other documents relating to the design, development, or manufacture of each register(s) used in writing, reading, buffering or accessing data from or to each cache memory used with, incorporated in or relied on by a Freescale Product.

REQUEST NO. 30:

All documents relating to drawings, schematics, blueprints, manufacturing specifications, engineering specifications, design specifications, product test specifications, part specifications, assembly specifications and other documents relating to the design, development, or manufacture of each cache controller used with, incorporated in or relied on by a Freescale Product.

REQUEST NO. 31:

All documents relating to drawings, schematics, blueprints, manufacturing specifications, engineering specifications, design specifications, product test specifications, part specifications, assembly specifications and other documents relating to the design, development, or manufacture of each process for forming conductors that include a layer of tungsten overlying a layer of titanium nitride used with or in, incorporated in or relied on by a Freescale Product.

REQUEST NO. 32:

All versions of operation manuals, repair manuals, or user manuals for any Freescale Product.

REQUEST NO. 33:

All manufacturing and/or production drawings for any Freescale Product,

including but not limited to hardware drawings, engineering drawings, assembly drawings, and blueprints.

REQUEST NO. 34:

All manufacturing and/or production drawings for each cache memory used with, incorporated in or relied on by any Freescale Product, including but not limited to hardware drawings, engineering drawings, assembly drawings, and blueprints.

REQUEST NO. 35:

All manufacturing and/or production drawings for each register(s) used in writing, reading, buffering or accessing data from or to each cache memory used with, incorporated in or relied on by a Freescale Product, including but not limited to hardware drawings, engineering drawings, assembly drawings, and blueprints.

REQUEST NO. 36:

All manufacturing and/or production drawings for each cache controller used with, incorporated in or relied on by a Freescale Product, including but not limited to hardware drawings, engineering drawings, assembly drawings, and blueprints.

REQUEST NO. 37:

All manufacturing and/or production drawings for each process for forming conductors that include a layer of tungsten overlying a layer of titanium nitride used with or in, incorporated in or relied on by a Freescale Product.

REQUEST NO. 38:

All documents relating to the conception, engineering, design, research, development, manufacture, testing, use, repair and/or operation of each version of each model of Freescale Product, including but not limited to specifications, schematics, block diagrams, data

sheets, layouts, databases, depictions, photographs, simulations, test results, manuals, journals, notes, notebooks, communications, and correspondence.

REQUEST NO. 39:

All documents relating to the conception, engineering, design, research, development, manufacture, testing, use, repair and/or operation of each version of each cache memory used with, incorporated in or relied on by any Freescale Product, including but not limited to specifications, schematics, block diagrams, data sheets, layouts, databases, depictions, photographs, simulations, test results, manuals, journals, notes, notebooks, communications, and correspondence.

REQUEST NO. 40:

All documents relating to the conception, engineering, design, research, development, manufacture, testing, use, repair and/or operation of each version of each register(s) used in writing, reading, buffering or accessing data from or to each cache memory used with, incorporated in or relied on by a Freescale Product, including but not limited to specifications, schematics, block diagrams, data sheets, layouts, databases, depictions, photographs, simulations, test results, manuals, journals, notes, notebooks, communications, and correspondence.

REQUEST NO. 41:

All documents relating to the conception, engineering, design, research, development, manufacture, testing, use, repair and/or operation of each version of each cache controller used with, incorporated in or relied on by a Freescale Product, including but not limited to specifications, schematics, block diagrams, data sheets, layouts, databases, depictions, photographs, simulations, test results, manuals, journals, notes, notebooks, communications, and correspondence.

REQUEST NO. 42:

All documents relating to the conception, engineering, design, research, development, manufacture, testing, use, repair and/or operation of each process for forming conductors that include a layer of tungsten overlying a layer of titanium nitride used with or in, incorporated in or relied on by a Freescale Product, including but not limited to specifications, schematics, block diagrams, data sheets, layouts, databases, depictions, photographs, simulations, test results, manuals, journals, notes, notebooks, communications, and correspondence.

REQUEST NO. 43:

For each Freescale Product, documents sufficient to show the place and process of manufacture, models manufactured, units manufactured, and destination of units manufactured.

REQUEST NO. 44:

To the extent not produced in response to any other request, all reference designs and schematics relating to each version of each model of Freescale Product.

REQUEST NO. 45:

All pictures or photographs of Freescale Products, including but not limited to any die or portion of any die.

REQUEST NO. 46:

Circuit diagrams for each version of each model of Freescale Product.

REQUEST NO. 47:

Circuit diagrams for each version of each cache memory used with, incorporated in or relied on by any Freescale Product.

REQUEST NO. 48:

Circuit diagrams for each version of each register(s) used in writing, reading,

buffering or accessing data from or to each cache memory used with, incorporated in or relied on by a Freescale Product.

REQUEST NO. 49:

Circuit diagrams for each version of each cache controller used with, incorporated in or relied on by a Freescale Product.

REQUEST NO. 50:

Process flows and process recipes for each version of each model of Freescale Product.

REQUEST NO. 51:

Process flows and process recipes for each version of each process for forming conductors that include a layer of tungsten overlying a layer of titanium nitride used with or in, incorporated in or relied on by a Freescale Product.

REQUEST NO. 52:

All documents relating to source code, object code, pseudo code, flow charts or design specifications of the circuit diagrams, Verilog code and/or VHDL code, and reticle layout code for each version of each model of Freescale Product.

REQUEST NO. 53:

All documents relating to source code, object code, pseudo code, flow charts or design specifications of the circuit diagrams, Verilog code and/or VHDL code, and reticle layout code for each version of each cache memory used with, incorporated in or relied on by any Freescale Product.

REQUEST NO. 54:

All documents relating to source code, object code, pseudo code, flow charts or

design specifications of the circuit diagrams, Verilog code and/or VHDL code, and reticle layout code for each version of each register(s) used in writing, reading, buffering or accessing data from or to each cache memory used with, incorporated in or relied on by a Freescale Product.

REQUEST NO. 55:

All documents relating to source code, object code, pseudo code, flow charts or design specifications of the circuit diagrams, Verilog code and/or VHDL code, and reticle layout code for each version of each cache controller used with, incorporated in or relied on by a Freescale Product.

REQUEST NO. 56:

Documents sufficient to identify the date of all revisions to circuit diagrams, source code, Verilog code and/or VHDL code, and reticle layout code for each version of each model of Freescale Product.

REQUEST NO. 57:

All documents relating to the operation of each version of each model of Freescale Product.

REQUEST NO. 58:

All documents relating to the operation of each version of each cache memory used with, incorporated in or relied on by any Freescale Product.

REQUEST NO. 59:

All documents relating to the operation of each version of each register(s) used in writing, reading, buffering or accessing data from or to each cache memory used with, incorporated in or relied on by a Freescale Product.

REQUEST NO. 60:

All documents relating to the operation of each version of each cache controller used with, incorporated in or relied on by a Freescale Product.

REQUEST NO. 61:

All engineering change orders or notices for each version of each model of Freescale Products.

REQUEST NO. 62:

Documents sufficient to show the device and system architecture of each version of each model of Freescale Product.

REQUEST NO. 63:

All documents relating to comparative testing of each version of each model of Freescale Products.

REQUEST NO. 64:

All prototypes and models of Freescale Products, from initial prototype to commercial and/or production models made from 2000 to the present.

REQUEST NO. 65:

Complete copies of all licenses or agreements to which you are a party, including but not limited to cross-licenses, inter-company agreements, settlements, covenants not to enforce or releases that relate in any way to integrated circuit manufacturing, microprocessor, microcontroller, DRAM, SDRAM or memory technologies.

REQUEST NO. 66:

All documents that refer to, discuss, evidence, mention or constitute any contracts or license agreements, including drafts, in which Freescale has licensed, or licenses, or

considering licensing products, technology or patents from or to third parties relating to microprocessor, microcontroller, processor or memory technologies.

REQUEST NO. 67:

All documents relating to your policies on licensing or cross-licensing patents, know-how or technology.

REQUEST NO. 68:

Documents sufficient to identify any third parties that manufacture any Freescale Products.

REQUEST NO. 69:

All articles, speeches, presentations or interviews, both internal and external, that have been written and/or given by your employees, officers, directors or other of your representatives relating to Freescale Products.

REQUEST NO. 70:

All press releases from 2000 to the present relating to Freescale Products.

REQUEST NO. 71:

All documents relating to ProMOS or the patents-in-suit, including but not limited to documents that relate to your first awareness of any of the patents-in-suit and your earliest notice of potential infringement of any of the patents-in-suit.

REQUEST NO. 72:

All documents relating to communications exchanged between you and any third party relating to the patents-in-suit, this lawsuit and/or ProMOS.

REQUEST NO. 73:

Each Freescale meeting agenda, corporate minutes or minutes of meetings relating to the patents-in-suit, this lawsuit and/or ProMOS products.

REQUEST NO. 74:

All documents relating to any effort by Freescale or anyone else on its behalf to design, redesign, commercialize or modify any Freescale Product in view of the patents-in-suit.

REQUEST NO. 75:

All documents relating to any attempt by Freescale or anyone on its behalf to design around and/or avoid infringement of the patents-in-suit by any Freescale Product.

REQUEST NO. 76:

All documents related or referring to any ProMOS patent.

REQUEST NO. 77:

All documents relating to your evaluation, analysis, or consideration of the patents in-suit, including but not limited to any reverse engineering or testing performed on any Freescale Product.

REQUEST NO. 78:

All documents relating to your consideration of whether or not to obtain a license from ProMOS for the patents-in-suit.

REQUEST NO. 79:

All documents found or identified during any enforceability, prior art or invalidity searches, or any other studies relating to the patents-in-suit, including any copies of patents, publications, or other prior art identified during such searches or studies.

REQUEST NO. 80:

All documents that relate, support, or contradict Freescale's assertion that the patents-in-suit are invalid for any reason, including but not limited to anticipation or obviousness.

REQUEST NO. 81:

All documents that Freescale contends constitute prior art to the patents-in-suit.

REQUEST NO. 82:

All documents that relate, support, or contradict Freescale's assertion that the patents-in-suit are unenforceable.

REQUEST NO. 83:

All opinion letters, memoranda, or other documents relating to your contentions on validity/invalidity, infringement/non-infringement, or enforceability/unenforceability of the patents-in-suit.

REQUEST NO. 84:

All documents supporting, refuting or relating in any way to the affirmative defenses or counterclaims set forth in your Answer to the Complaint.

REQUEST NO. 85:

All documents relating to any contention by you that your products do not infringe the patents-in-suit, including but not limited to documents relating to the interpretation, scope, and meaning of the claims in any of the patents-in-suit.

REQUEST NO. 86:

All opinions of counsel obtained with respect to infringement, validity, or enforceability of the patents-in-suit upon which you intend to rely at trial to defend against claims of willful infringement, inducement to infringe, or contributory infringement.

REQUEST NO. 87:

All communications or opinions of officers, directors and/or employees of yours with respect to infringement, validity, or enforceability of the patents-in-suit or regarding any licensing negotiations with ProMOS.

REQUEST NO. 88:

Documents sufficient to show by month or calendar quarter for each year since 2000 the number of each version of each model of Freescale Product manufactured, used, sold or distributed in the United States.

REQUEST NO. 89:

Documents sufficient to show by month or calendar quarter for each year since 2000 the volume of sales in dollars from the sale or distribution of each version of each model of Freescale Product.

REQUEST NO. 90:

All projections, forecasts, business plans, strategic plans, fiscal plans, marketing plans or sales plans relating to the sale of Freescale Products from 2000 to the present, including documents containing projections through calendar year 2012.

REQUEST NO. 91:

All documents relating to the means by which sales or sales information relating to each version of each model of Freescale Product is maintained and tracked by or on behalf of Freescale.

REQUEST NO. 92:

All versions of all part number decoders or legends for each version of each model of Freescale Product.

REQUEST NO. 93:

Current and historical price lists for each version of each model of Freescale Product.

REQUEST NO. 94:

All documents relating to returns of, or complaints, dissatisfaction, negative comments, unfavorable opinions or suggestions for improvement regarding each version of each model of Freescale Products.

REQUEST NO. 95:

All documents relating to favorable, positive, commendatory, or complimentary feedback, comments or opinions regarding each version of each model of Freescale Products.

REQUEST NO. 96:

All documents relating to favorable, positive, commendatory, or complimentary feedback, comments or opinions regarding any ProMOS product.

REQUEST NO. 97:

All documents relating to sales, distribution or importation agreements entered into between Freescale and any third party for each version of each model of Freescale Product.

REQUEST NO. 98:

Documents sufficient to show each of your distributors, resellers and customers of each version of each model of Freescale Product.

REQUEST NO. 99:

All documents relating to purchase orders and/or specifications received from customers or potential customers for each version of each model of Freescale Product, including all drawings and information received therewith.

REQUEST NO. 100:

All documents relating to market shares for Freescale and its competitors for each of the Freescale Products.

REQUEST NO. 101:

Summary documents categorized by year and by product type and name regarding the following: (1) Freescale's total unit and dollar volumes for Freescale Products manufactured, sold, or offered for sale by you from 2000 to the present, including projections through calendar year 2012; and (2) revenues, costs (fixed and variable), gross profit, and net profit for all such products manufactured, sold or offered for sale by you from 2000 to the present, including projections through calendar year 2012.

REQUEST NO. 102:

Summary documents categorized by year and by product type and name regarding gross expenses, including but not limited to direct labor costs, direct manufacturing costs, selling costs, variable overhead costs, incurred in the manufacture, distribution, or sale of Freescale Products from 2000 to the present, including projections through calendar year 2012.

REQUEST NO. 103:

Documents sufficient to show the date of the first sale of each Freescale Product.

REQUEST NO. 104:

Summary documents identifying the distributors and retailers to whom you have sold each Freescale Product from 2000 through the present, including the name, address, product(s) sold by model number, number of units sold, date of sale, date of shipment, and sales price.

REQUEST NO. 105:

Financial statements, including profit and loss statements, income statements, balance sheets, statements of cash flow, statements of retained earnings, and notes thereto for Freescale and any of its affiliates, divisions, subsidiaries, or parent companies.

REQUEST NO. 106:

All documents relating to market, industry or consumer studies, surveys, or analyses of any Freescale Product and/or any competitor's product.

REQUEST NO. 107:

All drafts, proposals, and final copies of advertising, sales, or promotional literature, including but not limited to television and print media advertising, brochures and trade show promotional material, catalogues, price lists, sell sheets, product descriptions, sales literature, drawings, videotapes, audio tapes, electronic media, or photographs for advertising, point-of-sale commercials, or other promotional material for Freescale Products.

REQUEST NO. 108:

All memoranda, correspondence, bulletins, newsletters, or other documents that currently or since 2000 have been distributed to, made available to, received from, or drafted by your present or former employees engaged in marketing or sales functions relating to Freescale Products.

REQUEST NO. 109:

All documents prepared by, provided by, sent to, or received from your advertising agencies or public relations firms relating to any Freescale Product.

REQUEST NO. 110:

All documents that you may introduce as exhibits at the trial of this matter.

REQUEST NO. 111:

All documents identifying by name, company, address and title, all third parties hired by you or your counsel to investigate the above-captioned litigation, ProMOS, the patents-in-suit, or any ProMOS products.

REQUEST NO. 112:

Ten samples of each Freescale Product.

REQUEST NO. 113:

Any and all witness statements taken in connection with this litigation.

REQUEST NO. 114:

All documents provided to any person(s) that you expect to call as an expert witness at trial.

REQUEST NO. 115:

All documents relied upon by any person(s) that you expect to a call as an expert witness at trial in forming the opinion(s) as to which the person(s) will or may testify.

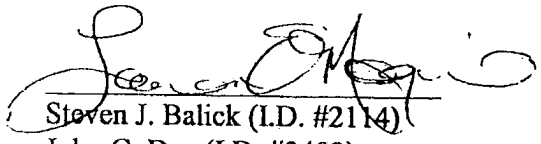
REQUEST NO. 116:

All documents relating to each person you employ, have employed, or have retained as an expert, including but not limited to curriculum vitae, resumes, retention agreements, letters, statements, and communications.

REQUEST NO. 117:

All documents on which you intend to rely for and/or that might be relevant to a reasonable royalty analysis or calculation using the so-called *Georgia Pacific* factors.

ASHBY & GEDDES



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Dated: April 12, 2007
179643.1

CERTIFICATE OF SERVICE

I hereby certify that on the 12th day of April, 2007, the attached **PLAINTIFF PROMOS TECHNOLOGIES, INC.'S FIRST SET OF REQUESTS FOR PRODUCTION OF DOCUMENTS AND THINGS FROM DEFENDANT FREESCALE SEMICONDUCTOR, INC. (Nos. 1-117)** was served upon the below-named counsel of record at the address and in the manner indicated:

Mary B. Graham, Esquire
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P.O. Box 1347
Wilmington, DE 19899-1347

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VIA FEDERAL EXPRESS

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Cleveland, OH 44114-1190

VIA FEDERAL EXPRESS

Lauren E. Maguire

177267.1

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC.,	)	
	)	
Plaintiff,	)	C.A. No. 06-788-JJF
	)	
v.	)	
	)	
FREESCALE SEMICONDUCTOR, INC.,	)	
	)	
Defendant.	)	

NOTICE OF SERVICE

The undersigned hereby certifies that on the 12th day of April, 2007, **PLAINTIFF PROMOS TECHNOLOGIES, INC.'S FIRST SET OF REQUESTS FOR PRODUCTION OF DOCUMENTS AND THINGS FROM DEFENDANT FREESCALE SEMICONDUCTOR, INC. (Nos. 1-117)** was served upon the following counsel of record at the address and in the manner indicated:

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/s/ *Lauren E. Maguire*

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Dated: April 12, 2007
177270.1

CERTIFICATE OF SERVICE

I hereby certify that on the 12th day of April, 2007, the attached **NOTICE OF SERVICE** was served upon the below-named counsel of record at the address and in the manner indicated:

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Cleveland, OH 44114-1190

/s/ *Lauren E. Maguire*

Lauren E. Maguire

Discovery Documents

1:06-cv-00788-JJF Promos Technologies Inc. v. Freescale Semiconductor Inc.
PATENT

U.S. District Court

District of Delaware

Notice of Electronic Filing

The following transaction was entered by Maguire, Lauren on 4/12/2007 at 12:33 PM EDT and filed on 4/12/2007

Case Name: Promos Technologies Inc. v. Freescale Semiconductor Inc.
Case Number: 1:06-cv-788
Filer: Promos Technologies Inc.
Document Number: 13

Docket Text:
NOTICE OF SERVICE of First Set of Requests for Production of Documents and Things From Defendant Freescale Semiconductor, Inc. (Nos. 1-117) by Promos Technologies Inc..(Maguire, Lauren)

1:06-cv-788 Notice has been electronically mailed to:

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EXHIBIT D

REDACTED

EXHIBIT E

REDACTED

EXHIBIT F

REDACTED

EXHIBIT G

REDACTED

EXHIBIT H

REDACTED

EXHIBIT I

REDACTED

EXHIBIT J

Handbook of Semiconductor Manufacturing Technology

edited by

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14

Physical Vapor Deposition

Stephen M. Rossnagel
IBM Thomas J. Watson Research Center, Yorktown Heights, New York

I. INTRODUCTION AND SEMICONDUCTOR APPLICATIONS

Physical Vapor Deposition (PVD) thin film technology covers a rather broad range of deposition techniques. The general feature that describes PVD is that films are deposited atomically by means of fluxes of individual neutral or ionic species. This differentiates them from Chemical Vapor Deposition (CVD), in which films are precipitated from the gas phase by a chemical reaction, and also from electrodeposition, in which atoms or ions in an aqueous solution are plated onto a surface.

PVD techniques include all techniques based on evaporative deposition, such as e-beam or hot-boat evaporation, reactive evaporation and ion plating. PVD techniques also include all processes based on sputtering, either by a plasma or by an ion beam of some sort. PVD is also used to describe deposition from arc sources which may or may not be filtered.

In the current day semiconductor industry, PVD technology is entirely based on physical sputtering, usually using a specific type of diode source known as a magnetron. Atoms are physically sputtered from the magnetron cathode by means of a local plasma, and the sputtered metal atoms are then used as the basis for film deposition once they travel to the location of the sample. The other PVD techniques, such as e-beam evaporation or ion beam sputtering, have been used in either the earlier days of semiconductor processing, or else exist on the fringe of development projects, and do not have any significant relevance to mainstream interconnect processing.

The primary semiconductor applications for PVD technology are the deposition of metal and compound lines, pads, vias, contacts and related connections which are used to connect with the junctions and devices present on the Si wafer surface. The emphasis here is on electrical connection: the PVD features are not part of the semiconductor junction directly, but make the electrical connections between it and nearby circuit features.

With the feature size of the desired metal structures decreasing with each succeeding semiconductor generation, the techniques to both pattern and deposit PVD features has evolved over the years. Aside from the very early days of photoresist-based lift-off deposition, there have been two primary lithographic pattern technologies used for PVD deposition. The first is a subtractive process based on the deposition of planar films and the subsequent patterning of features by means of Reactive Ion Etching (RIE) [1]. This will be called the "RIE-Metal" technology for this chapter (Fig. 1).

The second general class of deposition techniques uses an alternate approach where trenches and vias are etched into planar, dielectric film layers. These features are then filled with metal and polished flat, in a techniques known in the industry as "Damascene"

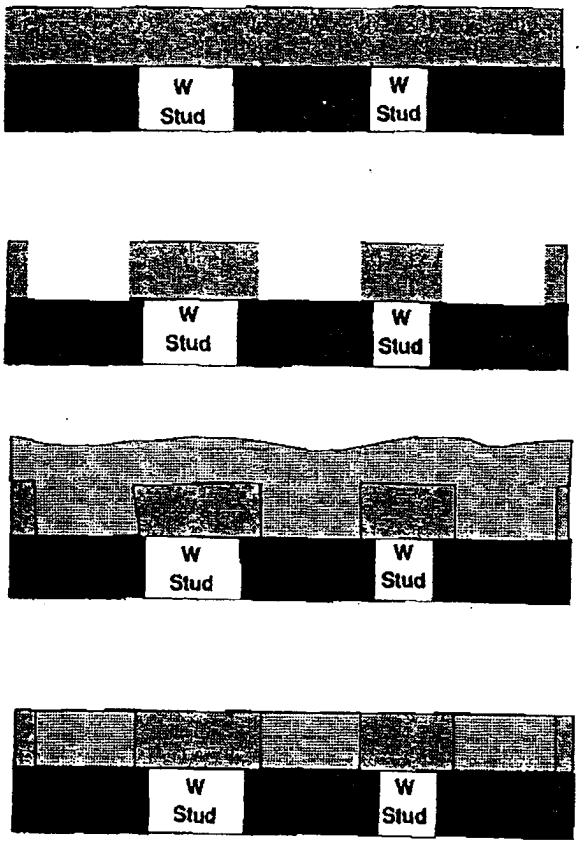


Figure 1 Sketch of several steps of the RIE-Metal patterning process.

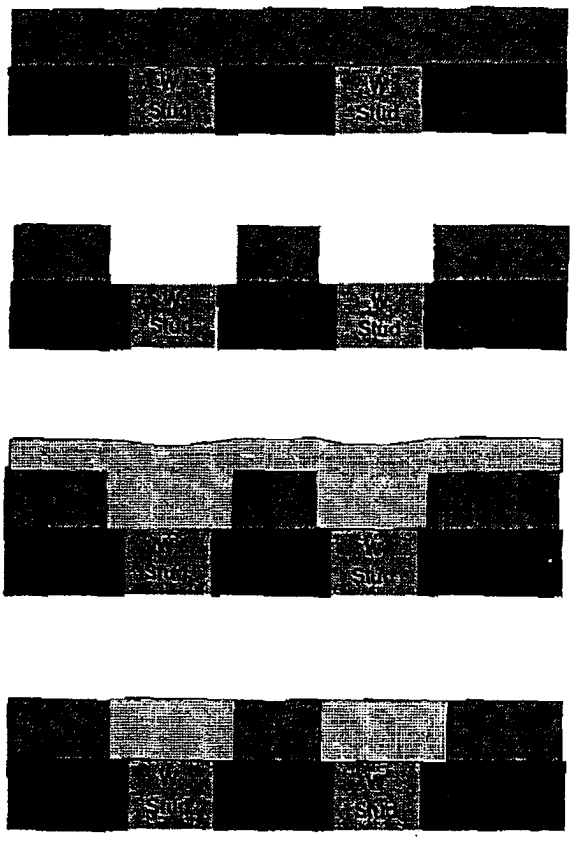


Figure 2 Sketch of steps used for Damascene metal filling technology.

processing, named after similar ancient jewelry making techniques (Fig. 2) [2].

The PVD technologies used for each technology: RIE-Metal, and Damascene, are completely different, as in one case there is a desire for a completely planar, flat film covering over small steps and bumps, and in the second case there is a need for a more directional or preferential deposition where the deposition occurs deep into features such as trenches and vias.

II. SPUTTERING BACKGROUND AND BASICS

For PVD techniques based on sputtering, the vast majority of the cases of interest will use bombardment of a negatively-biased cathode by means of a high energy, inert gas ion, typically Ar, but occasionally other inert gas species (Ne, Kr) or also occasionally reactive species such as oxygen or nitrogen. The physical sputtering process is well understood in the literature [3–8] and consists of a sequence of energetic, violent collisions between the incident particle and a cold lattice of the target (Fig. 3). The effect of this incoming ion is to physically dislodge one or more of the target atoms, which then in turn move on striking other atoms within the surface lattice structure. This near-cascade of collisions can eventually result in one or more atoms in the near surface layers having just enough kinetic energy (and the appropriate direction) to overcome the surface binding energy and escape. This escaping atom is then described as having being sputtered from the surface, although it may have originated 1–2 layers down from the original surface.

The exact sequence of collisions is, as might be evident from the sketch, very dependent on the exact trajectory and impact site of the incident ion. Since these are not controllable features, sputtering is usually described in terms of average effects: the result of many

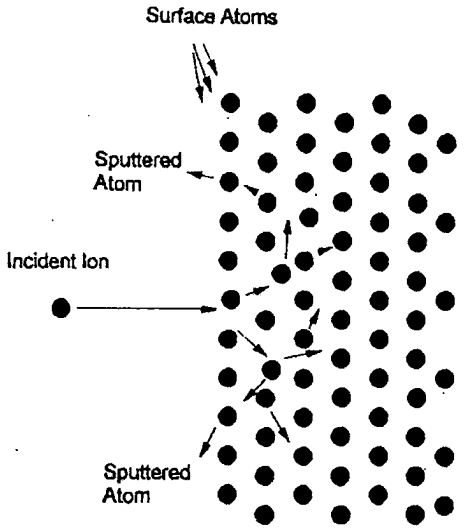


Figure 3 Schematic of sputtering event. (From Ref. 8.)

millions or more impacts by energetic ions and the average emission of sputtered particles from variety of lattice orientations. This is known generically as the sputter yield, and it is simply the ratio between the number of emitted, sputtered particles and the number of incident, high energy impacting ions. The sputter yield is generally a number which is based on both the kinetic energy of the incoming ion (as well as its mass) along with the species of the impacted surface. The yield varies from essentially undetectable at very low ion energies (10 s of eV) to numbers on the order of 1–5 at modest ion energies of many hundred to thousands of eV. A graph of the sputter yields for some materials of interest to semiconductor processing is shown in Figure 4.

The angular emission distribution of the sputtered atoms is characterized by a so-called cosine distribution in which the relative flux at any angle other than the surface normal scales with the normal-direction flux times the cosine of the angle from normal. There are numerous deviations from this general rule, and in general, lower ion energies tend to result in a flatter, "under-cosine" distribution whereas higher ion energies tend to result in a more peaked, over-cosine distribution [9]. There are also unusual cases where the crystal structure of the sputtered material can have an effect on the angular emission distribution. This was first observed in the 1950s by Wehner, who saw spots in the emission distribution characteristic of the underlying crystal structure [10]. More recently, preferential emission has been incorporated into

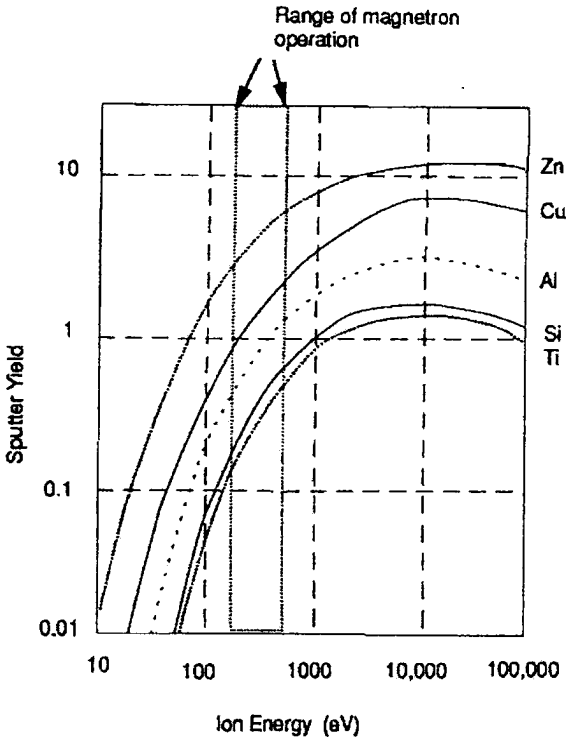


Figure 4 Sputter yields as a function of incident Ar ion energy for several materials. (From Ref. 8.)

magnetron target fabrication to produce an emission distribution which is much more peaked than the conventional cosine distribution [11].

The sputtered atoms must then move through the background gas to land at the desired sample surface. Most magnetron sputter deposition systems are operated at pressures in the low milliTorr range where the mean free path for gas-phase collisions is generally greater than the distance between the cathode and the sample, or throw distance. This means that most of the sputtered atoms will have ballistic trajectories with few, if any, in-flight collisions. At pressures above a few milliTorr, this no longer holds, and as the pressure approaches 30 mTorr or so, essentially all of the sputtered atoms have numerous gas-phase collisions and lose essentially all of their original kinetic energy and direction from the sputtering process [12–16]. This process is known as 'thermalization' from the point of view of the sputtered atom, which becomes thermally equilibrated with the background gas. The process also results in significant as heating, though, resulting in a local rarefaction of the background gas in the region in front of the cathode. For significant levels of applied

Table 1 Deposition probability for magnetron sputtering at 1000 W, 200 mm dia cathode planar magnetron [17].

Throw (cm)	Pressure (mtorr)	Deposition probability
Ar Sputtering of Cu		
5 cm	5, 20, 30	0.63, 0.49, 0.54
9.5 cm	5, 20, 30	0.48, 0.47, 0.45
14.5 cm	5, 20, 30	0.39, 0.35, 0.31
Ne Sputtering of Al		
5 cm	5, 20, 30	0.80, 0.56, 0.52
9.5 cm	5, 20, 30	0.40, 0.42, 0.40
Ar Sputtering of Al		
5 cm	5, 20, 30	0.60, 0.46, 0.42
9.5 cm	5, 20, 30	0.44, 0.45, 0.35
Kr Sputtering of Al		
5 cm	5, 20, 30	0.52, 0.45, 0.38
9.5 cm	5, 20, 30	0.35, 0.27, 0.22

Source: Ref. 17.

magnetron power, the resulting gas density can be as low as 20% of the starting density, with an equivalent gas temperature of 1500°K or more [17]. This sputter-induced change to the gas density can also be used in a model of the plasma discharge to predict the current-voltage trends of the cathode [18].

The efficiency of the transport process is partly dominated by operating conditions and partly by the design and configuration of the system. Since the emission process is essentially a cosine distribution and in most production tools the cathode diameter is not much smaller than the internal chamber diameter, significant deposition will occur on the chamber sidewalls as well as any fixtures such as shuttered, ground shields, clamp rings, etc. The probability of transport can be characterized by a number between 0 and 1, where 1 means that all sputtered atoms from the cathode land on the desired sample surface and 0 implies that no atoms are deposited [17]. Although rarely measured, the data shows expected trends with pressure, throw distance and gas used, as well as target species (Table 1). In this latter case, it is expected that when the target atomic weight exceeds the weight of the background gas that transport will be more efficient.

A more commonly used metric to characterize deposition efficiency is to calculate the unit deposition rate per watt of applied power. This is quite sensitive to the system used. The results are usually given in units of Angstroms/sec/Watt. An example of this type of data is shown in Table 2 for an Applied Materials Endura sputtering chamber (12.98 in cathode, 5 cm throw) [8,19]. In general, a typical number for this deposition efficiency is on the order of 1 Angstrom/sec/Watt, with higher numbers for materials such as Cu which have a high sputter yield.

Table 2 Deposition rates per watt and also deposition probability for Applied Materials Endura sputtering system. The cathode is 12.98 in dia (standard 200 mm size), the throw distance is 5 cm, and the samples are 200 mm Si wafers [20].

Materials	Power	Rate (Ång/min/watt)
AlCu (0.5)	12.7 kW	1 (new cathode) 0.75 (old cathode)
Ti	1 kW	0.17
TiN (nitride mode)	4 kW	0.15
Ti (collimated, 1.5:1)	7 kW	0.043

III. PVD SYSTEMS

PVD technology covers a lot of various non-chemical deposition techniques. For semiconductor applications, essentially 100% of the deposition systems are based on a variation of a dc-diode device known as a magnetron. There are occasionally reports of work done using rf-diode deposition systems, but these are usually used in cases of dielectric materials, such as the high-k dielectric, and are not in widespread usage. Readers interested in rf technology are referred to a review chapter by Logan of IBM [21].

A magnetron cathode differs from a conventional, planar cathode in that there is a local magnetic field parallel to the cathode surface. This is shown in Figure 5. The effect of the tangential B field is such that secondary electrons which are emitted from the cathode surface due to ion bombardment (which is what causes the sputtering), undergo an "E × B" drift around the cathode surface in a manner similar to the Hall Effect. These drifting electrons are trapped close to the cathode region and can lead to very high levels of gas ionization, which results in very large discharge (ion) currents.

The magnetrons used in semiconductor production systems derive from this basic design. The cathode diameter is typically 50% larger than the sample to be deposited on (30–32 cm for a 200 mm wafer sample). This scaling is likely to hold as wafers migrate

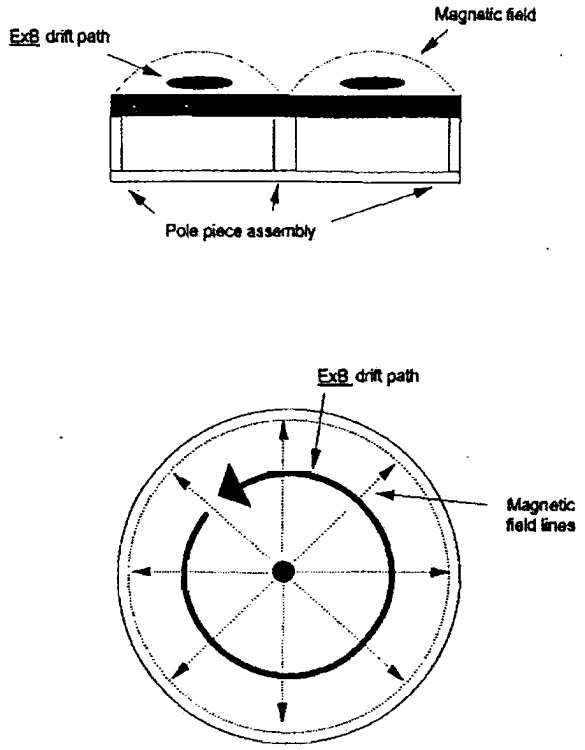


Figure 5 Schematic of acircular, planar magnetron cathode.

to the 300 mm generation, resulting in cathode diameters on the order of 45 cm. The cathode-to-sample distance, or 'throw' distance ranges from about 3 to 10 cm, with most tools operated at about 5 cm. In most production tools, the wafers are positioned horizontally, such that they are facing up, and the magnetrons are configured to sputter down onto the wafer. Originally there was concern that this configuration would result in the maximum particulate contamination of the sample, due simply to gravity. However, most sub-micron particles in vacuum systems are much more influenced by static charges, van-der Wahl forces, and gas-phase turbulence than they are by gravity.

The wafers are fixed on the substrate platforms in one of three ways: a physical clamp ring held down by either springs or gravity, no clamping at all with the wafer sitting up on small pins or pads, and electrostatic clamping. The use of clamp rings reduces the useful area of the wafer by several percent but tends to physically and thermally couple the wafer much better to the pedestal, giving moderate temperature control. Clampless operation gives full wafer coverage, but at the expense of any control whatsoever over the thermal or electrical condition of the wafer. Electrostatic clamping can give the best of both worlds, and many major tool suppliers are beginning to make low temperature, biasable e-chucks available [22]. A continuing concern over the use of electrostatic chucks is to be able to diagnose the no-wafer failure mechanism. This means a case where for some reason the wafer does not arrive in the deposition chamber and yet the deposition is turned on. Due to the electrical nature of the electrostatic chuck, a blanket metal deposition onto an uncovered chuck results in destruction of the chuck. A second e-chuck concern is the presence of backside particulates, which may be pushed into the backside by the strong chucking force. This can lead to significant chamber-to-chamber contamination.

Production magnetrons are configured with a moving magnet array, rather than the fixed magnets of Figure 5. As shown in Figure 6, the magnet assemble is located behind the cathode surface and sloshes around in the water cooling bath, rotating about the cathode centerline. The etch track is usually somewhat heart-shaped with the indentation at the top of the heart roughly on the cathode centerline. This etch track/magnet system is driven by an external motor to cycle around the cathode surface at several Hertz. The exact shape of the etch track can be tailored by adjusting the magnets or the pole pieces. Changing the shape of the etch track results in changes in the uniformity of the deposition, which may be desirable either because of the material used or else the specific geometrical configuration. For example, if the throw distance is increased then more sputtered atoms are lost to the sides of the chamber, resulting in a net reduction in rate as a function of radius. In this case, it may be necessary to adjust the etch track to increase the erosion rate near the edge of the cathode to compensate. Alternatively, the use of a collimator (described below) completely changes the requires erosion profile of the cathode. Each cell of the collimator functions as a tiny pinhole camera, imaging a surface of the cathode onto the sample. Therefore the etch uniformity in that case must be higher than the long-throw case. In each case, it is also possible to tailor the erosion uniformity of the cathode to provide a high level of cathode utilization. Rotating-magnet cathodes might typically use 50–70% of the high purity cathode material before they must be replaced. This is much different from the conventional cathode (Fig. 5) which may only use 15% of its material before the erosion track becomes too deep. Higher cathode

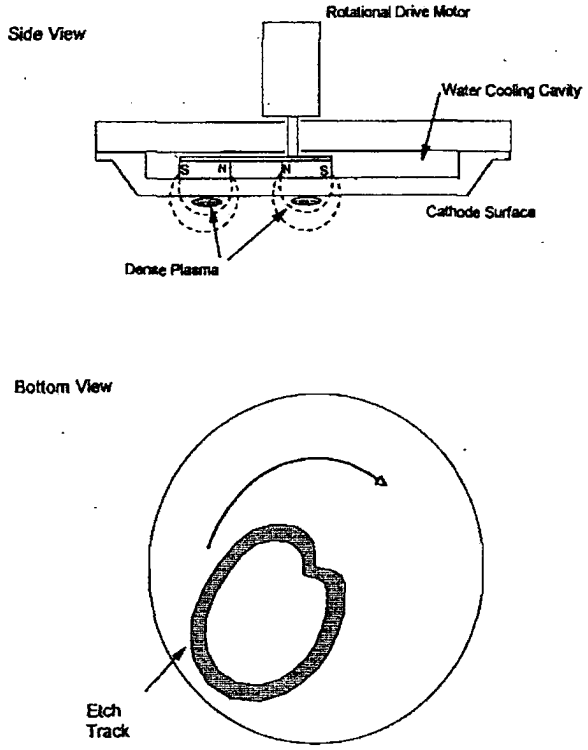


Figure 6 Magnetron design with moving-magnet, heart-shaped E x B etch track. (From Ref. 23.)

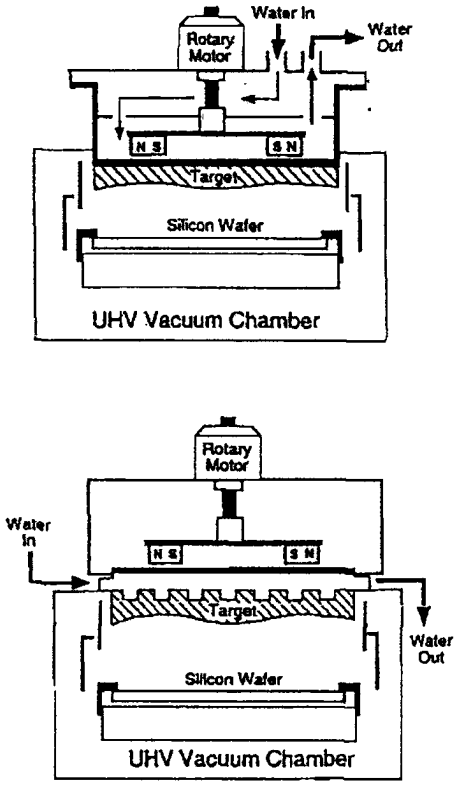


Figure 7 Magnetron cathode design with integrated water cooling channels. (From Ref. 23.)

utilization results in lower operating cost for the tool as well as longer times between cathode changes.

All magnetron cathodes are water cooled and the amount of cooling turns out to be the practical limit to discharge operation. This is quite unlike most other types of plasma devices, but in a magnetron the current-voltage interaction is such that additional discharge power is easy to add to the cathode in the form of amperes of ion current. The practical limit is when the cathode deforms or even melts. Practical and safety concerns limit the temperature of the cooling water at the cathode to 60°C or so. Assuming excellent heat transfer, this results in a requirement for about $\frac{1}{4}$ gallon-per-minute of water flow for each kW of applied discharge power. It has often been said that a magnetron sputter deposition system is simply a very expensive water heater.

Most commercial magnetron systems use a removable target-and-backing-plate assembly which is bolted to a non-conducting housing on which the motor drive is mounted. The cavity behind the cathode contains the magnets and also the cooling water, typically with water line of about 2 cm diameter. Recent cathode designs have migrated towards a target configuration which has built-in water channels (Fig. 7) [23]. This scales better to larger cathode size and allows the magnets to be operated in air rather than immersed in water, reducing the inevitable corrosion of both the magnets and the pole pieces. It does, however, make the target assemble more expensive. A conventional target-and-backing plate assembly for a 200 mm sample system might cost $3000 or so for moderate-purity AlCu or Ti.

The composition and purity of the target are obviously quite important to the deposition application. In the semiconductor industry, target composition is almost always described in the form of weight percent, which can differ significantly from atomic percent, which is used in traditional chemical analysis or chemical formulas. For example, $Ti_{0.8}$ $W_{0.2}$ is a compound composed of 80% Ti atoms and 20% W atoms. However, since the atomic weight of W is 3.8 x that of Ti, the weight percent of this compound is Ti(50)W(50), where the general nomenclature is that

weight percents are written with parenthesis. To further complicate the description, if one component in an alloy or compound is allowed with a trace amount of another material, the dominant percentage is often dropped. An example of this is AlCu(0.5), which has 0.5% by weight of Cu and 99.5% by weight of Al.

Target purity is described in terms of percent-purity, and from a practical point of view is always less than 100%. Typical purities for Al are 99.999% (5 9s) to 99.9995% (5 9s five), with lower purities for Ti (4–5 9s) and higher purities for Cu (6–7 9s). The purity for refractory materials is generally lower (3–4 9s) and these materials are not in widespread usage in semiconductor processing, yet. In all cases, though, a high purity disk of the desired material is typically diffusion bonded to an Al or Cu backing plate which is bolted to the magnetron cathode.

IV. APPLICATIONS AND VARIATIONS FOR INTERCONNECT APPLICATIONS

Semiconductor applications of PVD films tend to take two general approaches: planar films which are then etched using RIE technology, and fill-like applications, where the sample has trenches and/or vias etched into a planar surface.

A. Planar, Conductive, or ARC Films

Perhaps the widest usage of PVD films in the semiconductor industry is simply the blanket deposition of AlCu(0.5) metal layers. These films are deposited over planar surfaces or else surfaces with very low aspect ratio features. It is critical that the film be as flat as possible because the subsequent step is photolithographic exposure with a very shallow depth of field in preparation for subtractive etching. Typically, AlCu films are deposited at modest rate (a few thousand angstroms per minute) with a low level of wafer heating. This leads to grain growth in the films such that the grain size is comparable with the film thickness (1/2 micron level). The film orientation is typically (111).

A second widespread application of planar films is the deposition of TiN to form an Anti-Reflection Coating (ARC). This tailored film is used to optimize the photolithographic process, and may also play a role as either an etch stop or protective layer. Typically TiN films are deposited from pure Ti targets sputtered with a partial pressure of nitrogen. The nitrogen reacts with the Ti film atoms (at the sample surface) if the sample temperature is adequate, typically 250°C or so.

B. Reflow and Surface Mobility-Based Deposition

The fundamental problem of putting atoms into a deep feature can be solved in at least 2 ways: using either enhanced surface mobility of the deposited atoms, or else enhanced directionality of the atoms as they are deposited. The first mode is closest to the planar film applications discussed above and uses essentially the same toolset, although it does not address the fundamental, non-directional nature of sputter deposition. Two general techniques have evolved for addressing surface mobility of atoms: the first is simply increased sample temperature, and the second is based on a more macroscopic extrusion of film material into deep features.

The effects of increased sample temperature on film deposition include increased surface diffusion, grain formation and growth, increased chemical activity of the film material, and also somewhat negative features such as film agglomeration, void formation, re-evaporation, precipitation and interdiffusion of the film with underlying layers. The goal of a thermal reflow process is that atoms move from the planar or field areas of the sample towards inset or deep features, such as trenches or vias. Movement of these atoms means that their original deposition trajectory (and conditions) are unimportant, and this is consistent with conventional, high rate PVD magnetron deposition technology. Since the bottom of a via or trench has a concave shape, this will tend to be a sink for thermally diffusing atoms. However, this assumes that the trench remains open to the top during the reflow process. If the top is closed and a void formed, then subsequent atom motion is by means of bulk diffusion, rather than surface diffusion, and is characterized by a much higher activation energy. This means that at any given sample temperature, a bulk-diffusion-dominated process will be significantly slower than a surface diffusion process.

Thermal reflow was first applied to semiconductor filling in the late 1980s [24], and showed significant filling of low aspect ratio features in Al at temperatures around 500°C. It is generally required for reflow technology that the first layers of the film wet the underlying surface and have good adhesion, or else the effect of additional sample temperature will form clusters and droplets, rather than a continuous film. This is generally done with a 2-step process, in which

the seed layer is deposited at low temperature and the sample temperature is increased such that the remainder of the deposition is at high enough temperature to facilitate rapid reflow [23]. Several variations on this process include the use of collimated sputtering or long-throw deposition or even the use of a CVD layer for the seed layer. The latter process has been commercialized and may be advantageous in slightly reducing the high temperature required for reflow [25]. This physics behind any sort of advantage have yet to be explained, but may be related to subtle chemical effects, such as the presence of hydrogen in the film deposited by CVD.

Thermal reflow processes require high levels of cleanliness because surface contamination of the wafer or gas phase impurities such as oxygen or water may significantly impede the surface diffusion process. For the case of reflow Al, very small amounts of oxygen (pressure of 10^{-7} Torr) are sufficient to form small oxide islands with then impede diffusion. Thin layers of Ti deposited just prior to Al reflow can result in better wetting and reflow of the Al as well as better adhesion [26]. The Ti can then be incorporated into the Al as $TiAl_3$ due to the elevated temperature, and this can serve to reduce film stress and the possibility of electromigration-induced failure [23]. This $TiAl_3$ phase, however, has a high resistivity which can lead to increased line resistance.

Reflow processes have been successfully applied to both the Al and Cu interconnect systems [27], although several intrinsic concerns have become apparent. The first concern relates to the requirement that the via or trench remain open during the reflow process, such that the activation energy for surface diffusion, as opposed to bulk diffusion, is dominant. This limits both the deposition rate as well as the minimum size of the feature. The interplay is between the non-normal incidence of the sputter deposition process, which tends to form voids, and the rate of surface mobility, which tends to fill the smallest vias and trenches first and also keep them open. The tradeoff is determined by the highest acceptable substrate temperature, as high temperature results is faster diffusion. Typically, the rule of thumb for oxide-based semiconductor processing is a maximum temperature of 400°C, and that temperature will decline significantly as the newer, low-k dielectrics are introduced.

The second concern relates to both the size of the feature as well as the surface density of features on the wafer. Since it simply takes more time, and more atoms, to fill a large feature as opposed to a small one, the larger features will lag during the processing. This is, perhaps, not a critical problem because filling low aspect ratio, large features is not difficult using conventional PVD. In terms of feature density, though, the features in the middle of large patterns of features will tend to fill last simply because the supply of atoms is from the side areas, and these will be captured first in the outermost features in an array.

A variation on reflow technology that has been developed recently is known generically as 'high pressure filling' [28]. This process uses conventional sputtering of blanket films, followed by exposure of those films to extremely high static gas pressures of an inert gas, such as Ar. The key to this process is, unlike conventional reflow deposition, it is greatly desired to deposit the films in such a way that voids are formed within high aspect ratio features. The samples are then removed from the sputtering chamber and introduced into a high pressure chamber. The temperature is raised to around 400°C, and Ar is introduced into the chamber at a level of 600–700 atmospheres. The large pressure, coupled with the elastic nature of the Al at 400°C (0.75 of melting T), allows the Al films to be squeezed or pushed down into the vias (Fig. 8). There remains only a few mTorr of inert gas within the void, and this gas is incorporated in the final structure at the 0.1 ppm level.

C. Directional Deposition

1. *Long Throw*

Most PVD systems are designed for maximum rate, and have short throw distances. This also results in the fewest number of atoms lost to the chamber walls. By moving the sample farther away from the cathode an increasing fraction of the sputtered atoms are lost onto the sidewalls of the chamber [29–31]. This results in a net reduction in the deposition rate at the sample, and also results in a net change in the average directionality of the depositing atoms. Atoms which are sputtered from the target surface at low angles (i.e. far from normal incidence) are more likely to land on the chamber sidewalls than on the wafer sample. The atoms arriving at the sample are more likely to be closer to normal incidence than the conventional, short-throw deposition. This geometrical filtering process is known generically as 'long throw' sputter deposition. The process is limited in a practical sense by the operating pressure of the system and gas scattering. To reduce in-flight scattering, the mean free path for the sputtered atoms should exceed the throw distance. To have any significant degree of directional

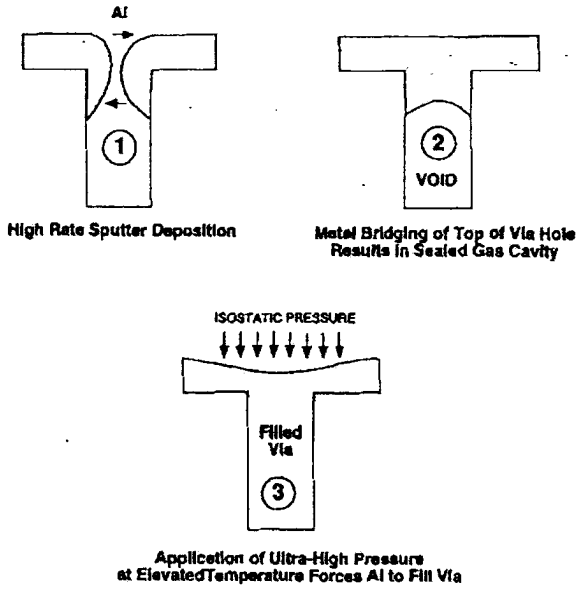


Figure 8 Sketch of the deposition process using high pressure extrusion. (1) high rate PVD deposition, (2) bridging or void formation, (3) application of high gas pressure resulting in movement of the metal film down into the via. (From Ref. 20.)

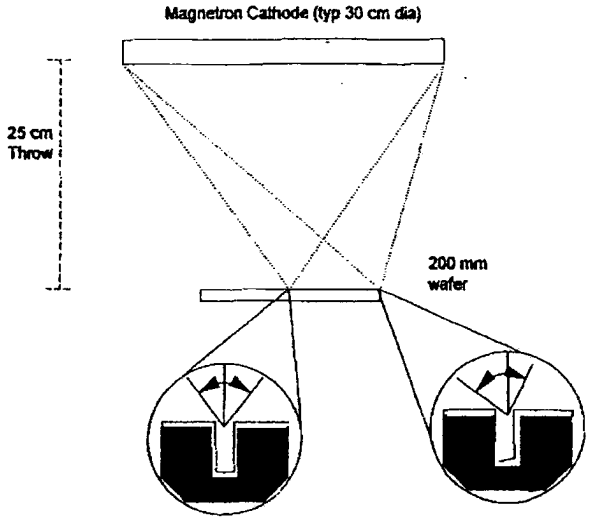


Figure 9 Sketch of center-to-edge asymmetry problem with long throw sputter deposition.

filtering, the throw distance needs to be on the order of the cathode diameter, of 25 cm for a 200 mm wafer system. This places a practical pressure limit of a few tenths of a mTorr on the operating pressure, as higher pressures will result in shorter mean free path distances than the throw distance.

Manufacturing applications of long throw deposition tend to have throw distances of about 25 cm, which limits the depositing flux to about ±45°. Greater directionality can only be obtained with longer throw distances, which require lower pressures. Most magnetrons will not operate below a fraction of a mTorr without some means of enhancement, such as a hollow cathode electron source [32].

Long throw sputter deposition is also limited by an intrinsic asymmetry problem, shown in Figure 9. In the case of a sample position near the centerline of the system, the deposition is uniform from all angles up to the cutoff angle. However, near the edge of the wafer, the deposition is stronger from the inner regions of the cathode, resulting in a greater buildup on the outer sidewalls of deep features (Fig. 10). The typical level of the asymmetry is 2–3×, and the ratio can be even higher at higher aspect ratio. Calculations as well as experiments have explored this

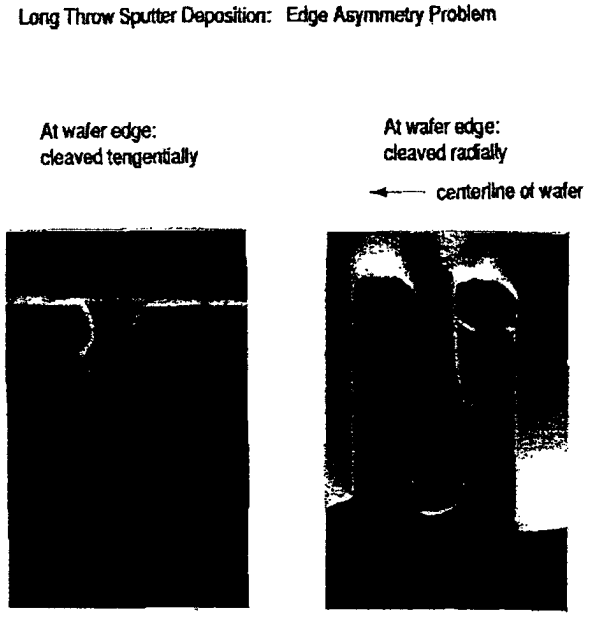


Figure 10 SEMs of vias located at the wafer edge showing the asymmetry of the depositing flux. Left side: a via cleaved in a direction parallel to the wafer edge, right side: a trench cleaved in the direction perpendicular to the wafer edge. (From Ref. 33.)

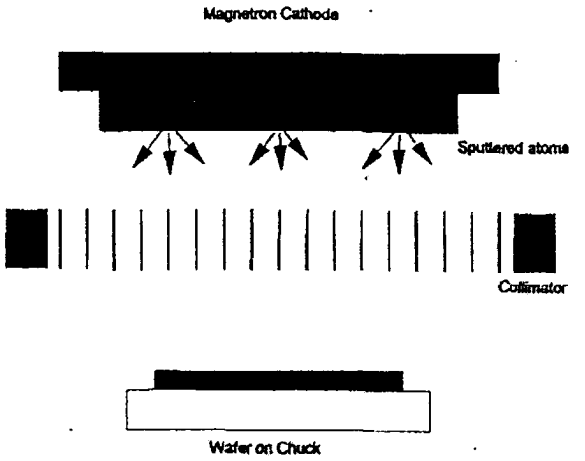


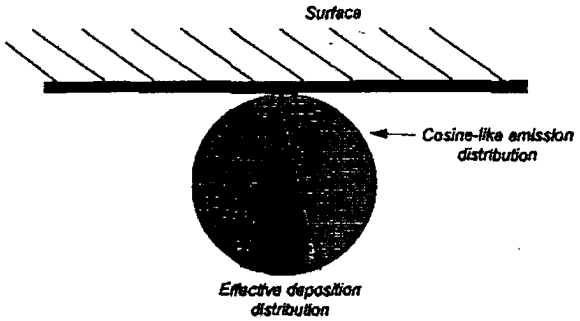
Figure 11 Collimated sputter deposition.

problem at length, but in reality there are no simple solutions other than increased throw distance.

Similar geometrical arguments limit the extendibility of long throw deposition to the 300 mm wafer generation. Since the cathode size scales up linearly (from 30 to 45 cm diameter), to attain the same level of directionality would require increasing the throw distance by 50%, and at the same time reducing the pressure by 2×. In general, this technology does not scale well to 300 mm and is unlikely to be commercially available.

2. *Collimated Sputtering*

In a long mean free path deposition environment (mean free path≫throw distance), geometrical filtering of the deposition flux can also be obtained by placing a collimator between the target and the sample [34–35]. The collimator serves as a simple directional filter by simply collecting the atoms which impinge on its walls. This is shown schematically in Figure 11. The degree of filtering is simply a function of the aspect ratio of the collimator, where aspect ratio is defined as the thickness of the collimator divided by the diameter of a cell. The effect on the sputtered flux is showing Figure 12, which shows the conventional emission distribution as a sphere centered about an impact site on the cathode surface. This sphere is the collection of all of the possible trajectories for the sputtered atoms. By increasing the aspect ratio of the collimator, the transmitted atomic distribution is shown as a cone centered about the surface normal. The higher the



For a 2 cm-high collimator located 2 cm from cathode:

Aspect ratio	*Emission width (degrees)*
1:1	*28 (i.e. +/- 14)*
2:1	*14*
3:1	*11*
4:1	*7*

Figure 12 Schematic of the emission distribution (shown as a sphere) and the subsequent filtering by a collimator.

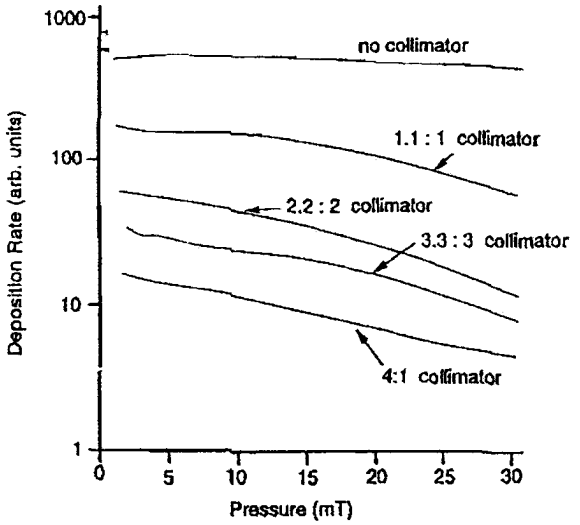


Figure 13 Deposition rate as a function of pressure through a variety of collimators.

degree of collimation, the smaller the half-angle of the deposited cone of material.

The deposition rate obviously suffers during collimated sputter deposition. For each 1 : 1 increase in the aspect ratio of the collimator, the deposition rate falls by about 3× (Fig. 13). Another way of picturing this is to consider the volume of the sphere in Figure 12, as compared to the volume of the cone of deposited material.

In collimated sputtering, it is generally not necessary to increase the throw distanee significantly, other than the thickness of the collimator (typically 2–3 cm) and perhaps another cm or so to prevent direct shadowing of the collimator sidewalls on the wafer. This points the throw distance at about 8–9 cm, which requires an operating vacuum in the 0.5–1 mTorr range such that there are few in-flight gas phase collisions. This operating pressure is within range for most commercial, production scale magnetrons.

Collimator designs have undergone several iterations the past 10 years. The original designs were machined from solid plates of Cu or Al: a close-packed hole pattern was machined by means of a numerically-controlled mill with sidewall thicknesses in the range of 40–50 thousands of an inch. The Cu or Al plates were water-cooled from the outer edge to prevent significant temperature buildup, although a center temperature of >100°C could be obtained. Eventually to increase the transparency of the collimator, the holes were machined with a hexagonal, rather than circular diameter. Current (late 1990s) collimators use spotwelded arrays of thin sheet metal (typically Ti or stainless steel) which drop into uncooled housings and are held without fixtures or screws. The use of Ti is desirable for collimated Ti depositions because of the match between the thermal expansion coefficient of the collimator and the deposited films. However, these uncooled collimators can also reach temperatures of 500°C during deposition, particularly of TiN.

Collimator lifetime is usually limited by eventual closure of the collimator cell, rather than flaking. The lifetime is roughly on the order of half of the target lifetime, but this depends strongly on the material used. Originally collimators were recycled and recleaned, but this is rarely done today in production. A sheet-metal collimator for a 200 mm tool costs $600–$2000.

3. *Applications*

Collimated sputtering was originally used for lift-off applications and then for filling trenches and vias [35]. Neither of these uses became practical commercially. In the semiconductor industry, collimated sputtering is mostly used for the deposition of Ti contact layers into the bottom of vias, and also for TiN diffusion barriers which are deposited prior to W-CVD. The bottom surface coverage (also known as "step coverage" is shown in Figure 14 as a function of the aspect ratio of the via. As expected, increasing

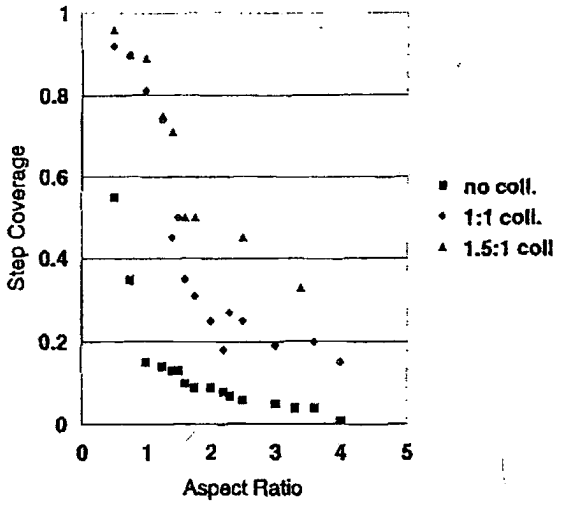


Figure 14 Bottom step coverage as a function of via aspect ratio for uncollimated, 1:1 and 1.5:1 collimated sputter deposition. (From Ref. 20.)

the aspect ratio of the collimator results in better bottom coverage and the technique appears to be adequate for aspect ratios of up to 4:1. Higher aspect ratios require ever increasing collimator aspect ratios, and manufacturing applications have tended to stay at the 1:1 or 1.5:1 level for practical reasons.

A somewhat unexpected application for collimated sputtering was its application for near-conformal diffusion barriers or "liners" [36]. This was not anticipated because collimated sputtering was viewed as a directional deposition technology, which should preclude any significant deposition on the sidewalls of features. However, during the early stages of a deposition, the function of the collimator is to prevent or reduce the intrinsic build-out of the deposit in the upper corners of the via. This allows additional deposition down the sidewalls and towards the bottom corner, more than would be anticipated by conventional deposition alone. However, this is only the case for the early stages of deposition as it is applied to a near-conformal film. As the films thicken, shadowing will rapidly cutoff deposition farther down in the feature. For semi-conformal deposition, acceptable results can be obtained with a collimator which has an aspect ratio significantly less than that of the feature.

From a practical point of view, these conformal films are less than ideal. There is a gradual taper from the upper corner to the bottom corner, and a significant crack at the bottom corner on all sides. In addition, the

film structure on the sidewalls is distinctly columnar, resulting in unwanted pathways for diffusion across the film. One solution to this problem has been to use multiple-step collimation, such that the film is split into two layers which hopefully do not have identical crystallinity (42). An alternate is stuffing the films with extra N or O to help make it more inert.

The filling of moderate aspect ratio features is possible with collimated sputtering [20,34] but rarely practiced. Filing has been demonstrated up to aspect ratios of 4:1, but this requires a collimator of equal to or greater aspect ratio. In addition, the sidewall deposits in the fill are underdense, similar to those observed with liner deposition, and this can provide poor resistance to electromigration. A second concern with filling applications is that it leaves behind a very think deposit on the field region of the wafer which must then be removed by means of CMP. This can add significant cost to the deposition process. An alternate scheme uses grazing-angle ion beam bombardment of the growing film (i.e. under the collimator) which can radically reduce the overburden and even reduce the amount of collimation required for good filling [37] This approach has not been extended to manufacturing, though, due to reliability concerns with broad beam ion sources.

D. Ionized Deposition

Physical sputtering is predominantly a neutral atom emission process: almost no ions are formed during the sputtering process, and even if an ion was formed, it would be held onto the surface by the electric field of the plasma sheath. Occasionally negative ions are formed in cases with very electronegative materials, but this is not an issue for almost all semiconductor materials [38]. The sputtered atoms are emitted with a wide range of angles, and since they are neutral, there is no other way than simple subtractive filtering to control their directionality.

In the late 1980s there was significant work in the field of high density plasma generation, primarily pointed towards etching applications. It became apparent during that work, though, that it was fairly easy to contaminate these plasma with metal atoms which had been sputtered, evaporated or arced from the internal walls of the system. These metal atoms were readily ionized and could be used to diagnose the etch plasmas. In general, though, this was considered a great nuisance since the metal ions would coat various insulating surfaces and windows in the high density plasma tools and ruin their effectiveness.

It was not long, though, before people began to intentionally introduce metal into their plasmas as a way of intentionally depositing films, this time from primarily metal ions as opposed to metal atoms. The intrinsic advantage of metal ion deposition is that due to the nature of the plasma sheath, which is parallel to the sample surface, all of the ions are deposited at exactly normal incidence. Regardless of the original trajectory of the metal atoms (which might have been sputtered off some nearby surface at a random angle), the metal ion was accelerated across the sample sheath at 90° and the kinetic energy was set completely by the difference between the plasma potential and the wafer potential, both of which can generally be easily controlled. These two features are the great, intrinsic advantages of ionized deposition, or as will be described in this chapter, I-PVD.

The earliest work used both sputtered and evaporated sources [39,40] and a high density plasma formed by Electron-Cyclotron Resonance (ECR) which is driven by a microwave source at 2.45 GHz. It is necessary to shield the entry point for the microwaves from metal deposition, and this was done by placing the window behind a bend. The tool is operated by initiating an ECR discharge in Ar, and then starting the evaporation source (typically Al or Cu). The metal atoms can then be ionized by the density inert gas plasma, and at some point the argon can be removed by pumping and the plasma sustained completely by the evaporative source. Since the sample location is not in a direct line-of-sight to the evaporative source, only ions are deposited. This system was used for direct, ionized deposition of Cu into semiconductor features at aspect ratios of 4:1 [40]. Unfortunately, there was little enthusiasm for reintroducing evaporation as a semiconductor process technology on the manufacturing scale, so this ECR approach has been converted to a physical sputtering approach [41,42].

In parallel with the high density microwave plasma work, there was also significant interest in inductively-coupled high density rf plasmas, typically operated at 1.9–13.56 MHz. Coupling this with metal based plasmas, early work was done by Yamashita [43] and also by Barnes, Forster and Keller [44] which combined a metal sputtering source with a dense, inert gas inductively coupled plasma which was used for metal ionization. Later work was extended to high rate manufacturing-scale sources as well as measurements of the basic plasma properties [45–47]. The general inductively-coupled rf approach to I-PVD is shown in Figure 15. The magnetron cathode is conventional,

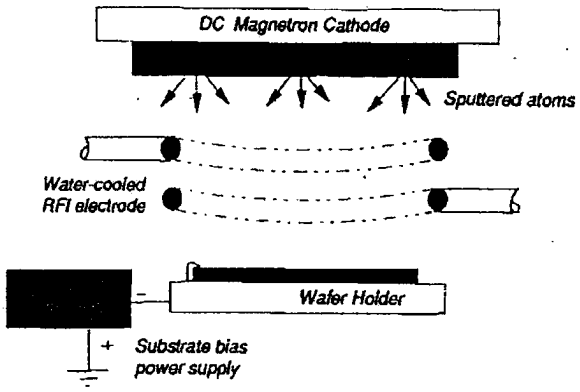


Figure 15 Experimental configuration for rf-based I-PVD. (From Ref. 20.)

i.e. it is the same cathode used for planar magnetron sputter deposition. In place of the collimator, a 1–3 turn rf coil is positioned approximately equidistant from the cathode and the sample, typically 3–4 cm from each. The coil diameter varies depending on the supplier and the group, and tends to be approximately the same diameter or slightly larger then the magnetron target diameter. It is most important that the coil not intercept the direct line-of-sight from the edge of the magnetron cathode to the sample, as this will result in shadowing near the wafer edge.

The function of the rf coil is to set up a dense, inductively coupled plasma in the background gas, which is typically Ar. The function of the magnetron is to sputter atoms into this discharge. At the sample, typically the sample potential is held by means of a clamp ring which, along with the sample pedestal, can be powered either rf or dc to a level of a few hundred watts at most. The wafer potential will typically be negative, and this will accelerate ions from the plasma, which has a positive plasma potential of a few volts, to the wafer. Using an rf bias overcomes problems with insulating wafer surfaces (or backsides), but results in an inability to measure actual sample currents.

The rf coil in early work was constructed of Cu tubing, and water cooling was supplied through the cooling to control the temperature. Coils of many sizes and dimensions were explored: varied numbers of turns, spiral coils, etc. The best results tend to come with a minimum number of turns (1–2) and the largest diameter tubing. These both tend to maximize the level of inductive coupling to the plasma, resulting in the highest plasma density. The rf coil, since it is exposed to the plasma, also develops a negative dc bias, typically of a few hundred volts. This can result in coil sputtering, even though the coil also receives a significant deposition flux from the plasma. By varying the tuning of the coil it is possible to operate the coil anywhere from a net deposition mode to a net etching mode. The former case allows the usage of a Cu coil for materials other than Cu, since the Cu will be buried under the depositing film. However, this film may also flake off over time resulting in particulate contamination. Operating the coil in the etch mode eliminates this problem, but requires that the coil be constructed from high purity material, since its atoms will be mixed in the discharge with the metal atoms from the magnetron, both going together to form the film. Commercial implementations of this approach have tended also to use non-water-cooled coils, since fabrication of water cooling in many materials (Ti, Ta, etc.) is nontrivial. The coil then runs hot, which may have negative effects on the film properties in some materials sets, particularly Al and Cu.

The relative ionization in the I-PVD rf system has been measured by using a gridded energy analyzer at the sample location. In place of a planar collector, the detector used a quartz crystal micro balance (Fig. 16). This allows the detector to differentiate between inert gas ions and metal ions. The data from this type of detector is not directly related to the relative ionization level in the plasma because the presheath tends to pull metal ions to the sample. However, it is consistent with the depositing flux ionization ratio.

The relative ionization, as might be expected, tended to increase as chamber pressure was increased

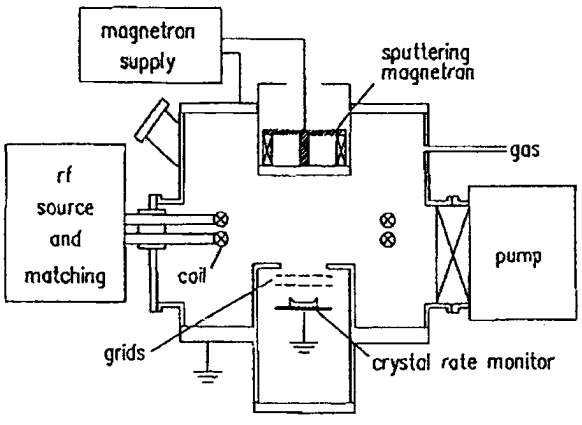


Figure 16 Retarding grid energy analyzer used to measure relative ionization of the deposition flux. (From Ref. 46.)

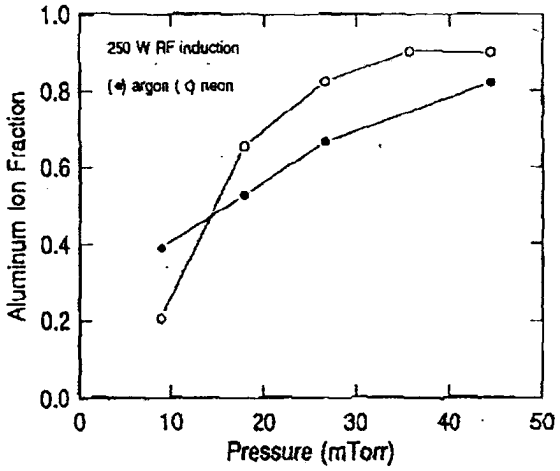


Figure 17 Relative ionization at the sample location for inductively-coupled I-PVD as a function of increasing pressure. (From Ref. 46.)

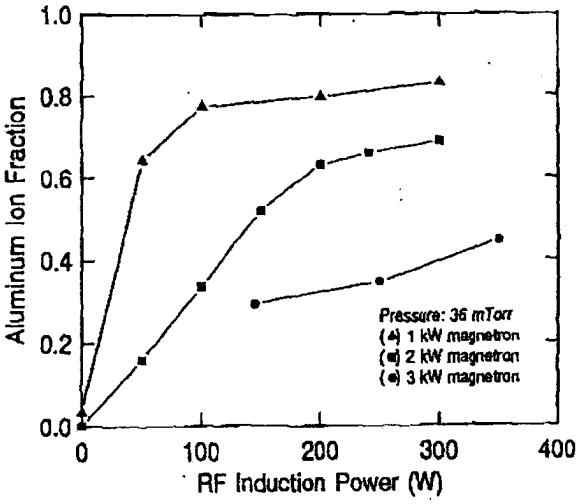


Figure 18 Relative ionization at the sample location for rf-based I-PVD as a function of chamber pressure for Ar and Ne. (From Ref. 43.)

to the inductively coupled discharge (Fig. 17). There was a slight different from Ar to Ne which may be attributable either to a higher electron temperature for Ne, or perhaps Penning ionization effects. However, it can be seen from the figure that relative ionization levels of 80–90% are possible. The maximum ionization was observed at pressures in the tens of mTorr range. At these pressures, the sputtered atoms tend to have many collisions in the gas phase, and as such, tend to stay the longest in the plasma region.

The relative ionization was also measured as a function of increasing rf power to the inductively coupled coil, as shown in Figure 18. In this case, the magnetron was operated at three different power levels, and these levels would scale approximately with the amount or number of metal atoms added to the discharge. At low metal fluxes (1 kW magnetron power), the ionization could be sustained at over 80%. However, as the metal flux was increased, the relative ionization was suppressed and could not be recovered by simply adding increased rf power. This was also observed in the ion current measured at the sample: increasing the metal flux to the plasma resulted in a reduction of sample ion current, consistent with a reduction in either plasma density or else electron temperature [48].

This general effect is quite troubling, because it is indicative of a less efficient plasma ionization process as the magnetron power is increased: something that is not favorable to high power scaling of the technology. Since the ion flux to a surface is directly proportional to the plasma density, which was assumed to increase as the more-easily-ionized metal was introduced to the plasma, it was thought that the plasma temperature (actually the electron temperature) was cooling significantly. However, experiments to measure this did not show significant cooling and actually showed a slight decrease in plasma density, even though the added metal atoms should have been much easier to ionize than the background, inert gas atoms.

This paradox was resolved by the development of a quantitative discharge model by Dickson, Qian and Hopwood [49]. The model was able to predict the various contributions to the ionization and plasma density from both electron bombardment as well as Penning ionization processes. The model was useful at some predictions of the discharge properties, but in its original development was unsuccessful at exploring significant increases in metal flux. However, they observed that if they allowed the gas density to decrease due to sputter-induced gas heating, the model correctly predicted the changes in discharge properties with added metal. This breakthrough was based on the earlier observations [17] of gas rarefaction and heating during magnetron sputtering. An example of this data is shown in Figure 19, which shows how the increased number of hot, sputtered metal atoms results in a measurable decrease in the gas density in the plasma region.

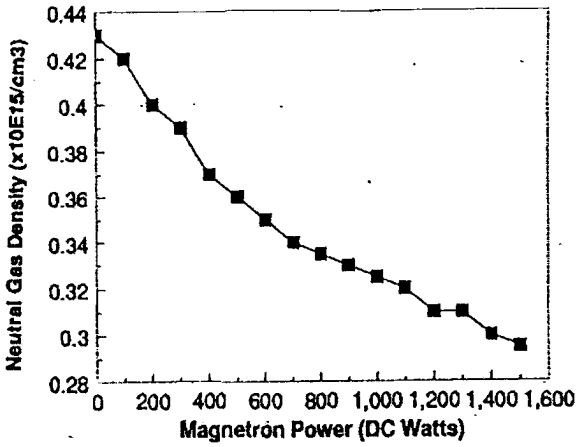


Figure 19 Change in neutral gas density at a fixed rf induction power of 1200 W as a function of increased magnetron discharge current. (From Ref. 20.)

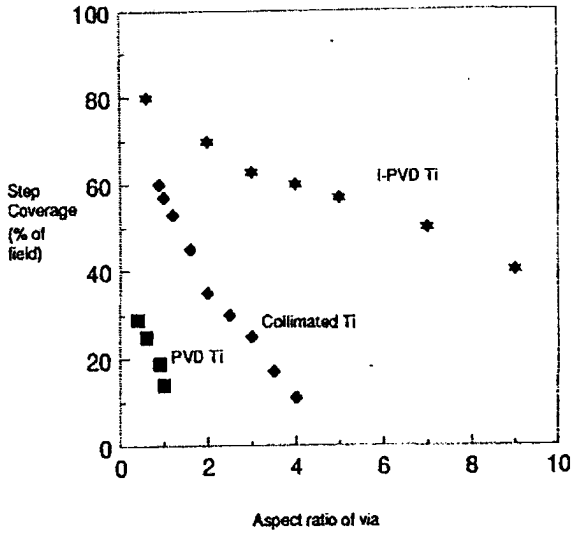


Figure 20 Bottom surface step coverage as a function of aspect ratio for conventional PVD, 1.5:1 collimated PVD, and I-PVD. (From Ref. 20.)

The model that emerges is as follows. As metal atoms are sputtered into the inductively-coupled, high density inert gas plasma, some of these metal atoms transfer their kinetic energy to the background gas. The result of the gas heating (in an open chamber) is that the gas density declines slightly. As this density drops, the amount of time that a sputtered atom spends in the plasma region declines slightly because the region is more transparent. And therefore, the likelihood of ionization of the metal atom is reduced. Adding more metal atoms to the discharge simply exaggerates the effect. It is almost as though the additional metal atoms result in a decreasing operating pressure, which according to the data of Figure 18, results in a less efficient ionization process. Several solutions exist, although the most obvious is to scale the inert gas density with the magnetron power such that the central gas density is fairly constant as more metal is introduced.

1. *Applications*

In many ways, I-PVD technology has very similar applications to the previously-described directional depositions based on filtering. By using the directional nature of the flux, depositions can be more easily made into deep, high aspect ratio features on semiconductor wafers. The three primary applications of this are bottom-contact layers, conformal coatings, and filling applications.

1. Contact layers. I-PVD techniques are ideal for projecting metal ions down to the bottom of a high aspect ratio via. In this application, the role of the deposited metal may be to make better electrical contact with some underlying contact or line, or else perhaps to deposit a metal for chemical incorporation into an under layer, such as a silicide of Ti or Co. The bottom step coverage (relative thickness as compared to the top, field thickness) as a function of aspect ratio is shown in Figure 20, comparing conventional PVD, collimated PVD and I-PVD [20]. As can be seen from the figure, high coverages of 50% or so can be observed at aspect ratios of 10:1. The step coverage declines slightly as the aspect ratio is increased due to small angle scattering across the sheath as well as small levels of ion temperature (fraction of eV) in the plasma. Actually, as a general rule of thumb, the relative ionization of the deposit can be inferred from the bottom step coverage at an aspect ratio of about 3:1. At smaller aspect ratios, there is a contribution to the bottom step coverage from the neutral deposition. At higher aspect ratios, scattering starts to become important.
2. Liners, diffusion barriers, adhesion layers and seed layers. One of the unexpected advantages of collimated sputtering was its usefulness at

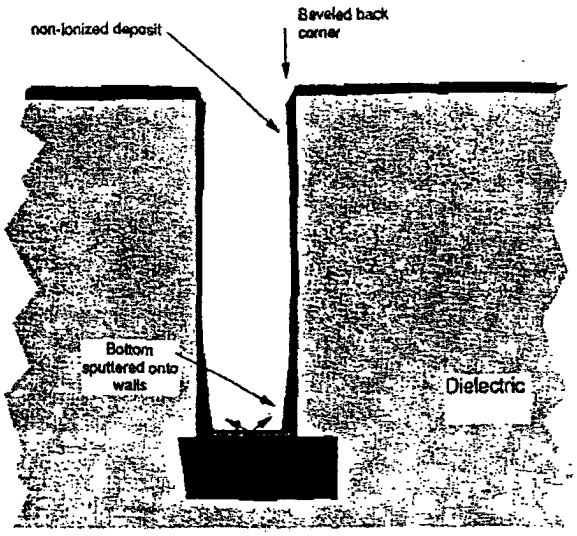


Figure 21 Sketch of I-PVD deposition of a line showing the effects of resputtering of the deposited film.

creating nearly-conformal coatings on the sides and bottoms of moderate aspect ratio features. This was unexpected because the collimated technology was intended to provide a more directional deposit, and conformality is generally inconsistent with high levels of directionality. I-PVD as a deposition techniques is in many ways similar to collimation: the flux is mostly directional with a bit of scatter. So the initial expectation is that it would be similar to collimated sputtering.

It turns out that there is a distinct advantage of I-PVD over collimated sputtering for near-conformal films. This advantage is related to the ability to control the depositing ion's kinetic energy, usually by simply adding a negative bias to the sample. The result is that the ion energy can be increased sufficiently to cause physical sputtering, or resputtering of the deposited films [50]. When this occurs with a liner film, two advantages are seen (Fig. 21). The first is that a small bevel forms at the top corners of the deposit, due simply to the fact that most materials have a slightly higher sputter yield at 45° or so than at normal incidence. This small bevel can taper back the overhang formation a little and tends to keep the via open. The second advantage occurs at the bottom of the feature, where atoms are sputtered from the bottom surface. These atoms are emitted with a cosine distribution and tend to end up depositing on the lower sidewall regions. The result is a slight thickening of the bottom corner deposition, which was exactly the place where the collimated deposition was weakest. This tapers in the bottoms corners a little and makes subsequent filling of the via even easier.

This process of local resputtering can be used to tailor the conformality of the deposit to a great degree. The process has been easily extended to aspect ratios of 5:1, and may extend to 7:1. Unfortunately, as the aspect ratio increases, the number of atoms or ions incident on the aperture of the via does not increase, and the result is an ever-thinner coatings.

3. Filling of trenches and vias. The goal of filling for trenches and vias is to provide high density, low resistivity metal with the desired microstructure and orientation. Somewhat like collimation, I-PVD alone will not turn out to be completely successful. Since the deposition on the sidewalls differs from the bottom deposit by being much more columnar and lower density, both collimated depositions or I-PVD depositions will need to be annealed at some fraction of the metal melting point to provide adequate recrystallization of the deposit.

I-PVD filling can be quantified by measuring the relative deposition rates on the sidewalls and bottom [48]. This data suggests that without additional sample temperature filling is limited in a practical sense to an aspect ration of about 2:1. Resputtering can be used at lower aspect ratio to taper back edges (Fig. 22), but as the aspect ratio is increased, sputtering results in local redeposition across the trench, resulting in void formation (Fig. 23).

V. SUMMARY, FUTURE DIRECTIONS

PVD technology has been one of the primary deposition techniques used for the manufacturing of semiconductor devices. Sputter deposition is used at almost all levels in the interconnect formation process, either in the form of thin films such as contact layers, diffusion barriers or seed layers, or for the primary conductors. The RIE-metallization process (Fig. 1) was ideally suited for PVD, as the requirement was for smooth, planar films which were continuous over

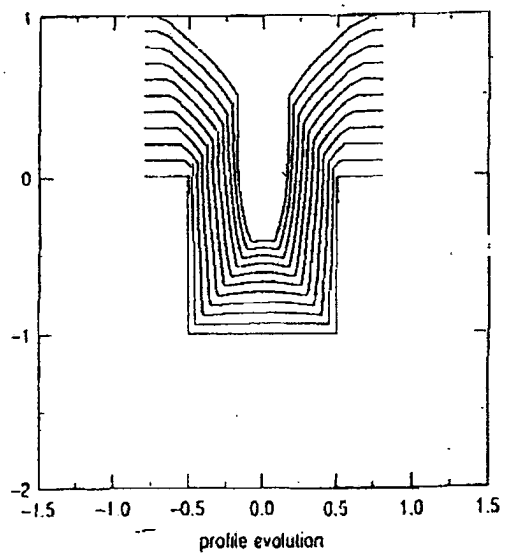


Figure 22 Computer simulation of the effect of resputtering at a feature aspect ratio of 1:1.

small steps or lines on the sample surface. The other widespread usage of PVD in semiconductor manufacturing is for the Ti bottom layers and TiN diffusion barrier layers in vias, often deposited using collimated sputtering, which were then subsequently filled with W using a CVD process. These technologies have been adequate for semiconductor generations down to the 0.35 micron-width level.

As the feature size continues to decline and as the aspect ratio of the interconnect features continues to increase, it is obvious that conventional PVD or even filtered PVD (collimated or long throw) will not be adequate techniques due to the poor step coverage at high AR and the overhang formation. This has led to the I-PVD techniques, as well as continuing work in CVD technologies and electroplating as eventual replacements for PVD.

CVD technologies have some additional degrees of flexibility that are not present with PVD. For example, depending on the sample temperature, the gas dynamics, and even the substrate surface composition, CVD films can be deposited with almost 100% conformality at very high aspect ratio. In addition, CVD film composition and purity can also be controlled by adjustments to the process gas or the sample temperature. Most of the materials relevant to interconnect technology: Al, Cu, Ti, TiN, W and TaN can be deposited by CVD, generally in a temperature and environment which is compatible with wafer processing.

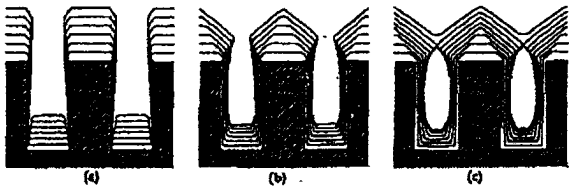


Figure 23 Simulations of the effect of increasing levels of resputtering n filling, using a 50% relative ionization. The sputter yield for (a) was 0, for (b) was 0.4, and (c) was 1.0. (From Ref. 51.)

There are several challenges, though, with CVD technology which has limited its widespread usage for all materials aside from W-CVD. For example, Al CVD has been demonstrated but only for pure Al, whereas the semiconductor industry requires small levels of Cu doping in the films for electromigration resistance. It is possible to get around this by depositing a thin layer of CVD-Al, followed by a PVD AlCu, which after a subsequent temperature cycle the PVD material donates some of its Cu to the CVD-Al layer. This is a variation on the two-step reflow process described above, and is available commercially. The conformality of the CVD-Al is useful at high aspect ratio as a seed layer for the subsequent, conventional PVD reflow deposition. A similar technique has been developed for CVD-Cu: a thin seed layer of CVD-Cu followed by an elevated temperature Cu reflow deposition using conventional PVD.

CVD techniques for Ti and TiN are often constrained by the presence of impurities, generally from the precursors. CVD-Ti, which is typically deposited from $TiCl_4$, can have trace Cl levels in the deposited film. The TiN, deposited from either a TDMAT or TDEAT precursor at temperatures in the 400°C range can have significant levels of C or O in the films, which can partly be alleviated by a nitrogen plasma treatment. The resulting films, though, have significantly higher resistivity than PVD films. In general, CVD technologies are characterized by increased cost and complexity, as well as subtle chemical problems, compared to equivalent PVD techniques such as collimation or I-PVD.

Electroplating has also become viable as a potential interconnect deposition technique for Cu applications for filling high aspect ratio vias and trenches. (Electroplating is not practical for Al deposition.) Since Cu rapidly interdiffuses into Si forming deep traps, Cu is unlikely to be used for the first layer of metallization (M-0); those vias which contact the wafer

surface will most likely remain as CVD-W. However, in the upper interconnect layers, Cu's lower resistivity compared to AlCu makes it an ideal candidate for higher speed lines and vias. Since Cu can diffuse into the dielectric (although at a much slower rate than into Si) it is necessary to use a refractory diffusion barrier, such as TiN, TaN, or W. It may also be necessary to use an adhesion layer, such as Ti, Ta or Cr, as Cu does not adhere well to many surfaces, such as silicon dioxide. Finally, to reliably plate onto the sample surface, a seed layer of Cu is needed.

The conformal nature of the diffusion barrier, adhesion layer (if used) and seed layer can be addressed with either I-PVD films or CVD techniques. Since the aspect ratio of mid- and upper-level lines and vias is not likely to exceed 5 : 1, it is probable that I-PVD techniques will become widely used for these films, due to lower cost and the intrinsic simplicity of the I-PVD tools. Commercial tools have recently been announced, and are just beginning to reach the manufacturing floor. It is also apparent that I-PVD techniques will completely replace collimated PVD at the 300 mm wafer generation. The efficiency and cost of I-PVD deposition is significantly better than collimation.

I-PVD techniques are likely to be widely used for contact, barrier, adhesion and seed layers, but it is less clear if I-PVD will be used as a practical, cost-effective primary conductor. While there has been hesitation to consider electroplating as a legitimate semiconductor manufacturing process, there may be significant cost and performance advantages for electroplated films. While I-PVD filling techniques have been demonstrated at modest aspect ratios, significant work remains to be done to determine whether it can become a cost-effective technique for Cu. Since PVD-based manufacturing tools will continue to be needed for the various barrier and seed layers, I-PVD Cu filling may prove cost effective in that it resides on the same tool base and can easily be integrated with the prior layers, as opposed to a separate plating platform.

The nearing transition to 300 mm wafer diameter provides a number of challenges to the interconnect technology area. Aside from the obvious increase in the physical size of the deposition and etching systems, such topics as increased uniformity or reduced particulate counts will need to be addressed. PVD systems are well-placed to make the transition to 300 mm. The scaling of the magnetron cathode is a complex, but fairly-well understood technology, and much larger cathodes have been built for other industries such as flat panel displays or glass coating. The increase in cathode diameter, as mentioned above, will scale as roughly 1.5 × the wafer diameter, although the cathode-to-sample distance will remain constant at 4–10 cm. This means that the tools will become effectively even more two-dimensional and edge effects and the presence of chamber walls or tooling will be less important.

For directional sputter deposition, it is unlikely that either collimated sputter deposition or long throw deposition techniques will be widely used at 300 mm, and may not even be commercially developed. The I-PVD technology, based on the inductively-coupled rf-coil approach, has been demonstrated at 300 mm sample diameter, and is most likely to be the dominant process used. Depending on the approach used: either rf coil or Faraday shielded coil, the dimensions of the tools will be modified slightly. This is necessary to account for the presence of a significant sputtered flux from the coil in the etched-coil mode, or the capturing effect of the Faraday shield, reducing the edge plasma and metal density near the shield. However, there is significant latitude in the design of the magnetron cathode emission pattern to compensate for these two issues.

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EXHIBIT K

Plasma-assisted chemical vapor deposition of titanium nitride in a capacitively coupled radio-frequency discharge

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A new type of plasma reactor for the plasma-assisted chemical vapor deposition (PACVD) of titanium nitride (TiN) was designed and built. The reactor uses a rf discharge operating at a pressure ~1 mbar and at a frequency of 13.56 MHz. The dependence of various properties of the coating produced on the deposition parameters is studied in detail. Besides a determination of the thickness of the coating different analytical techniques such as Auger electron spectroscopy (AES), x-ray diffraction (XRD), and scanning electron microscopy (SEM) have been used to characterize the coating. In order to investigate mechanical properties of the deposit, Vickers hardness and critical load have been determined. TiN coatings of excellent quality have been deposited on all surfaces of objects of complex geometry. The quality of these coatings is equivalent to the quality obtained by classical CVD and physical vapor deposition (PVD) techniques. The deposition temperature of 500 °C permits the coating of hardened steel tools.

I. INTRODUCTION

Coating with a hard material is nowadays common practice for the improvement of the performance of many kinds of tools. Titanium nitride (TiN) is most widely used for this type of application. Even if the conventional chemical vapor deposition (CVD) process[1,2] is most commonly used today, plasma-based so-called physical vapor deposition (PVD) techniques[3,4] are continuously gaining importance. CVD offers an excellent uniformity of the deposited film, but the high deposition temperature is a major drawback (~1000 °C for TiN). With PVD techniques like sputtering or ion plating the deposition can be performed at low temperature (below 500 °C). To achieve good film uniformity it is necessary to rotate the working pieces in the vacuum chamber during the coating procedure. Plasma-assisted chemcial vapor deposition (PACVD) offers a combination of interesting advantages of both types of process, that is deposition at moderate temperature with good film uniformity without movement of the samples. A few works attempting to prepare TiN films by this technique have been reported previously,[5–12] but some problems are still unsolved.

II. EXPERIMENTAL DETAILS

A. Deposition apparatus and preparation of the coatings

The PACVD apparatus is shown schematically in Fig. 1. The reaction chamber was a steel vessel with a diameter of 320 mm and a height of 300 mm. The samples were situated on a substrate holder of high transparency in the middle of the reactor, which has also been used as the rf electrode. The plasma of the capacitively coupled rf discharge was mostly limited in the space between the upper and lower grounded counter electrode and the wall of the vacuum chamber. The feed gas was introduced into the reaction volume through a shower on the upper electrode. After passing the substrates, the gases flew down along the reactor wall and were exhausted through a pumping port in the bottom part of the reactor.

The discharge was maintained by a rf generator at a frequency of 13.56 MHz and a power of up to 2500 W. An automatic matching network is used to match the power supply impedance to that of the gas discharge.

Argon (Ar), hydrogen (H_2), nitrogen (N_2), and titanium tetrachloride ($TiCl_4$) vapor were used as a reactive gas mixture. The purities of the permanent gases were 99 999%, whereas the purity of $TiCl_4$ was only 99.5%. The $TiCl_4$ vaporizer has the design of a washing flash and uses Ar as a carrier gas. A ratio of 50:1 between Ar and $TiCl_4$ was selected by adjusting the temperature and total pressure of the vaporizer. Gas lines for the Ar–$TiCl_4$ mixture were heated to prevent condensation. The flow rates of all process gases were controlled by mass flow controllers. The main components of the gas mixture were Ar and H_2 with only small amounts of N_2 ($<10\%$) and $TiCl_4$ ($<1\%$).

Process pressures in the PACVD reactor ranging from 0.5 to 5 mbar are achieved by a roots blower plus rotary vane pump and are controlled with a throttle valve. Pressure measurements have been made with a diaphragm-type gauge.

There is no additional heating installed in the reactor. The temperature of the samples is a result of the supplied rf power and the losses. The temperature of the substrate electrode was measured by a thermocouple installed in its interior. Because of the strong rf interference during deposition, the measurement was carried out at the end of the deposition procedure.

A full deposition cycle was performed in the following way. After cleaning with acetone, the samples were mounted in the reaction chamber. Molybdenum and very smoothly polished cemented carbide plates have been used as substrates. After installation of substrates the reactor was evacuated to 10^{-3} mbar and backfilled with Ar to ~0.2 mbar.

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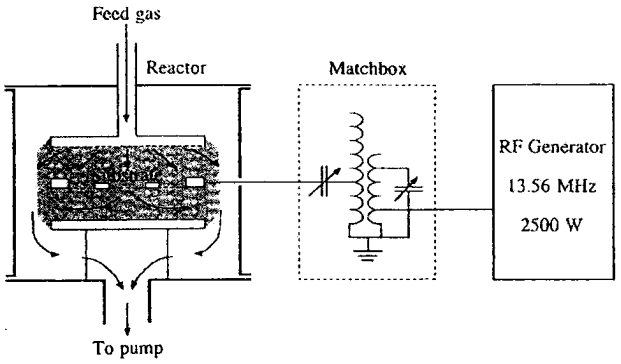

FIG. 1. Apparatus for plasma-assisted CVD using a rf discharge.

The samples were further cleaned by gas discharge for 15 min. The gas flow of the process gases, the total pressure and the rf power were adjusted to the desired values. After a reaction time of 1 h the discharge was stopped, all valves controlling the reactants were closed and the reaction chamber was evacuated. After cooling in a H_2 atmosphere the samples could be taken out of the chamber.

B. Analysis techniques for the characterization of the coatings

Compositional analysis of the coatings to determine the nitrogen-to-titanium (N/Ti) atomic ratio and the content of impurities (e.g., ratio of C/Ti, O/Ti, Cl/Ti) was carried out using Auger electron spectroscopy. For this purpose a commercial Physical Electronic Auger System (PHI 10-260) with a double-pass cylindrical mirror analyzer (CMA) and a single-electron counting detector has been used. The analyzer was operated in constant $\Delta E/E$ mode. The relative resolution of the analyzer is $\sim 1.6\%$ with the orifices used. The primary electron beam has been set to an energy of 8 keV and a primary electron current below 1 μA, yielding a count rate of several MHz at the detector. As the whole system is computer controlled, spectra have been recorded in the $N(E)$ mode and differentiated numerically. Prior to analysis, the system was baked to ~ 150 °C for several hours and pumped down to a base pressure of 2×10^{-10} mbar. Subsequently the system was filled with krypton to a total pressure of 5×10^{-5} mbar. In this atmosphere the samples were sputter etched for 15 min with an ion gun using a rastered 3-keV ion beam with a current density of ~ 150 nA/mm^2 to remove impurities from the surface. It has been reported by Sundgren,[3] that preferential sputtering occur in the Ti–N system. At substoichiometric compositions (N/Ti < 1) titanium is preferentially sputtered, whereas nitrogen is sputtered preferentially at overstoichiometric compositions. Sundgren has demonstrated, that in his case the N/Ti ratios obtained from AES of sputter cleaned surfaces have been up to 10% to high for substoichiometric coatings and up to 10% to low for overstoichiometric coatings. As even small amounts of impurities in the sputter gas have an influence on the apparent composition of the same sample,[13] the composition of the sputter gas has been observed by a quadrupole mass spectrometer.

Phase identification and preferred orientation of the coatings were determined by x-ray diffractometry (Philips type PW 1050/80) using CuK_α radiation. The morphology of the coatings was determined by investigation of the fracture cross sections using scanning electron microscopy (Jeol type JSM 35CF). The fractures were produced by breaking coated molybdenum substrates in liquid nitrogen. The mechanical properties, Vickers hardness (HV) and critical load, were determined on the deposited polished cemented carbide plates. Microhardness of the coatings was determined using a Vickers hardness tester at a load of 20 g. The indentations were measured with a filar eyepiece. Three measurements were taken from each sample. The average values have been determined and used to characterize the microhardness. The coating adhesion is characterized by a scratch test performed on a Rockwell hardness testing unit. The test essentially consists of drawing an indenter across the coating surface with various loads. The resulting scratches are observed under an optical microscope, by which minimum or critical load at which delamination of the coating occurs, is estimated and used as a measure of adhesion. The colors of the coatings were investigated by human eye and were described only in a subjective manner.

III. RESULTS

With the new reactor TiN coatings of excellent quality could be deposited on all surfaces of objects of complex geometry at moderate temperature (450 to 550 °C). This good uniformity of the deposited film could be achieved by a well-designed gas distribution system ("shower"). A more detailed discussion of this behavior is given elsewhere.[14] Excellent quality of the TiN coating means, that a dense δ-TiN phase of high hardness (2500 HV 0.02 to 3000 HV 0.02), low chlorine content, and with a sufficient critical load (~ 35 N) could be produced. A deposition rate of $\sim 3\,\mu$m/h could be achieved. It should be mentioned, that the most significant difference to TiN coatings produced by conventional PVD techniques, which indicates complete absence of chlorine in the coating, is the small residual chlorine content.

A. Effect of the N_2 concentration in the process gas

The deposition conditions for these investigations are given in Table I along with color, the phases present and the preferred orientation of the deposited TiN_x coatings. The N_2 concentration in the process gas has almost no influence on the self-bias dc voltage on the substrate.

1. Composition/stoichiometry

In Fig. 2, typical Auger spectra of the deposited TiN_x coatings are displayed. The spectra indicate films with only small amounts of impurities. Only in the case of the pure Ti coating the level of the impurities is remarkable (e.g., O/Ti = 0.03, Cl/Ti = 0.09), whereas in the case of TiN_x coatings the oxygen content was below the detection limits, the C/Ti and Cl/Ti ratio was below 0.02. The Cl/Ti ratios have been determined by using sensitivity factors of the

TABLE I. Color and structural data of the TiN_x coatings as a function of N_2 concentration in the process gas. Further process parameters which were kept constant: $TiCl_4$ concentration 0.14%, H_2 concentration 50%, pressure 1.50 mbar, rf power 2250 W, self-bias dc voltage − 300 V.

Notation	N_2concentration in process gas (%)	Phases present	Preferred orientation of δ-TiN	Color
TiN-1	0.00	α-Ti	···	Grey
TiN-2	0.35	α-Ti + ε-Ti_2N	···	Silver
TiN-3	0.70	ε-Ti_2N	···	Silver
TiN-4	1.05	ε-Ti_2N + δ-TiN	(200)	Silver
TiN-5	1.40	δ-TiN	(200)	Silver/gold
TiN-6	1.75	δ-TiN	(200)	Gold
TiN-7	2.10	δ-TiN	(200) + (220)	Gold
TiN-8	2.45	δ-TiN	(220)	Gold
TiN-9	2.80	δ-TiN	(220)	Gold
TiN-10	3.50	δ-TiN	(220)	Brown

"Handbook of Auger Electron Spectroscopy,[15]" whereas the C/Ti and O/Ti ratios have been determined by using a polycrystalline TiC standard and a TiO_2 standard. As already described in some earlier publications[4,16,17] the determination of the N/Ti ratio by AES has some difficulties, because of the near overlap of the N $KL_{23}L_{23}$ (at 380 eV) and the Ti $L_3M_{23}N_{23}$ and $L_3M_{23}M_{23}$ (at 383 and 387 eV, respectively) peaks and a Ti–N cross transition affecting the shape of the Ti $L_3M_{23}M_{45}$ peak (at 418 eV). The round robin experiment of Perry *et al.*[17] shows that the method described by Dawson and Tzatzov[16] deliver good results. In this work we evaluate the spectra with a quite similar method described by Laimer *et al.*[4] For this purpose the ratio of the Auger peak-to-peak heights of the peak at 385 eV and the peak at 418 eV of pure titanium (Ti-Std) and titanium nitride with a known composition (TiN-Std) have been determined. As no TiN crystal standard was available to us, a commercial available TiN coating with high hardness produced by reactive ion plating (RIP) has been used as a standard. It was estimated that the N/Ti ratio was ~1.00. With the used resolution of the spectra the resulting constants are $k_{\text{Ti-Std}} = I(385\text{ eV})/I(418\text{ eV}) = 1.16 \pm 0.04$ for pure titanium and $k_{\text{TiN-Std}} = I(385\text{ eV})/I(418\text{ eV}) = 2.47 \pm 0.04$ for the titanium nitride standard. The N/Ti ratio of the unknown sample can be calculated from the Auger peak-to-peak heights by using the following equation:

$$\left(\frac{N}{Ti}\right)_{\text{sample}} = \frac{(N/Ti)_{\text{TiN-Std}}}{k_{\text{TiN-Std}}}\left[\frac{I_{\text{Sample}}(385\text{ eV})}{I_{\text{Sample}}(418\text{ eV})} - k_{\text{Ti-Std}}\right].$$

The results are shown in Fig. 3. We can see, that the nitrogen content of the coating (as reflected in the ratio N/Ti) increases when the concentration of N_2 in the process gas is increased. At low N_2 concentrations the rise is strong, later it levels off and at ~2% N_2 concentration a saturation level of $N/Ti \approx 1$ is reached. As already mentioned in Sec. II B, the true N/Ti ratio can be lower in the substoichiometric range and higher in the overstoichiometric range as the evaluated

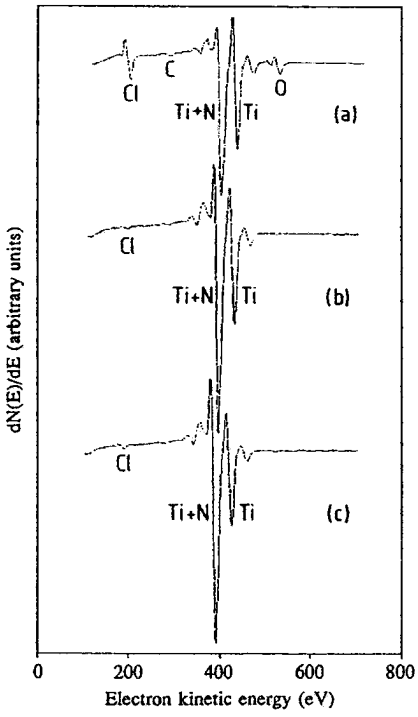

FIG. 2. Auger spectra of (a) TiN-1: single-phase α-Ti, (b) TiN-3: predominant ε-Ti_2N phase, and (c) TiN-5: single-phase δ-TiN illustrating the change in the appearance of the spectra in dependence of the N content.

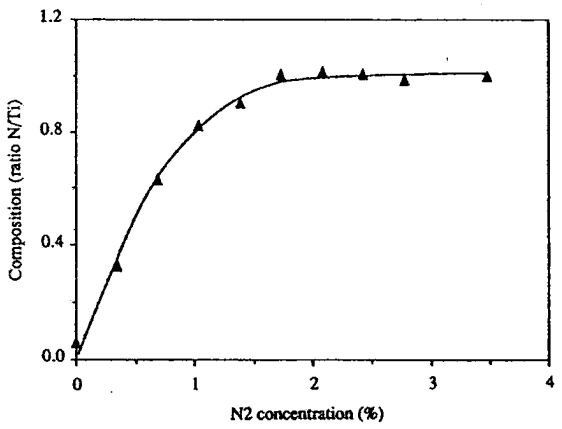

FIG. 3. Effect of N_2 concentration in the process gas on N/Ti ratio.

compositions suggest. A similar behavior (N/Ti ratio versus N_2 partial pressure) has been reported by Mayr *et al.* for PACVD in a dc plasma.[10] It is remarkable, that in absence of N_2 in the process gas the chlorine content of the coating is much higher.

2. Phases present and preferred orientation

Several phase diagrams of the Ti–N system have been published.[18–20] They exhibit besides β-Ti(N), which is stable only at elevated temperature, α-Ti(N), ϵ-Ti_2N, and δ-TiN_x. Recently more accurate investigations especially close to the composition corresponding to the ϵ-Ti_2N phase have been performed to determine the range of stability of the different phases.[21–25]. Figure 4 shows the results according to Ref. 24. Besides the new high-temperature phases ζ-Ti_4N_{3-x} (Refs. 22, 24, and 25) and η-Ti_3N_{2-x} (Refs. 23 and 25) a metastable compound δ'-$TiN_{0.50}$ as an intermediate step in the phase transition δ-$TiN_x \rightarrow \epsilon$-$Ti_2N$ was found.[24,25] Until now only α-Ti(N), ϵ-Ti_2N, and δ-TiN_x could be observed in coatings consisting of titanium and nitrogen.[3,26–31] It seems, that there are some uncertainties about the range of stability of the different phases in thin Ti–N films produced by plasma-assisted techniques. Although Sundgren reported,[3] that the phases present agree with the bulk phase diagram within the limits of error, Molarius *et al.* have reported,[26] that they have found α-Ti up to 38 at. % N and ϵ-Ti_2N up to 39 at. % N according to several identified reflections. Also δ-TiN_x could be observed up to 60 at. % N.[32–35] Because of the notoriously difficult exactly quantitative analysis of Ti–N films only a few papers are dealing with such investigations.[3,26] Many authors could not determine the composition exactly enough[27] or they have not investigated the correlation of phases present and composition.[31] According to the few published results it can be concluded, that the phases and the composition at which they occur may vary depending on processing details.

The data on phases present and preferred orientation of δ-TiN coatings of the investigation under consideration are shown in Table I. For some selected TiN_x coatings the XRD spectra are shown in Fig. 5.

As already reported in the case of sputtered TiN_x coatings, the lattice parameters can differ very strongly from bulk values and also from values of other coatings with the same composition.[17] Also the continuous shift of the x-ray diffraction peaks with increasing nitrogen content in combination with the strong anisotropy and possible peak overlap makes the identification of the peaks in some cases difficult.[3,26] In our case especially the peak at a diffraction angle of $\sim 62°$ cannot be identified without ambiguity.

The phases present in our TiN_x coatings depend on concentration of N_2 in the process gas used during deposition. It was observed that a single-phase α-Ti was formed at zero N_2 concentration [Fig. 5(a)] and a mixture of α-Ti and ϵ-Ti_2N phases at low N_2 concentrations. With a further increasing of the N_2 concentration ϵ-Ti_2N phase becomes predominant [Fig. 5(b)], later a mixture of ϵ-Ti_2N and δ-TiN phases and finally single-phase δ-TiN is observed [Fig. 5(c)]. Special attention should be given to sample TiN-4 (Table I), which exhibits a coating with only a small amount of ϵ-Ti_2N. This coating should be therefore on the lower limit of single-phase δ-TiN.

In TiN_x coatings produced by PACVD by other authors no ϵ-Ti_2N phase was found.[9] Molarius *et al.* report in the

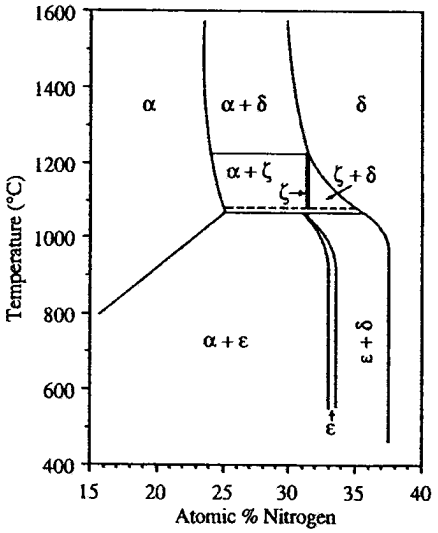

FIG. 4. Phase diagram of the Ti–N system (Ref. 24).

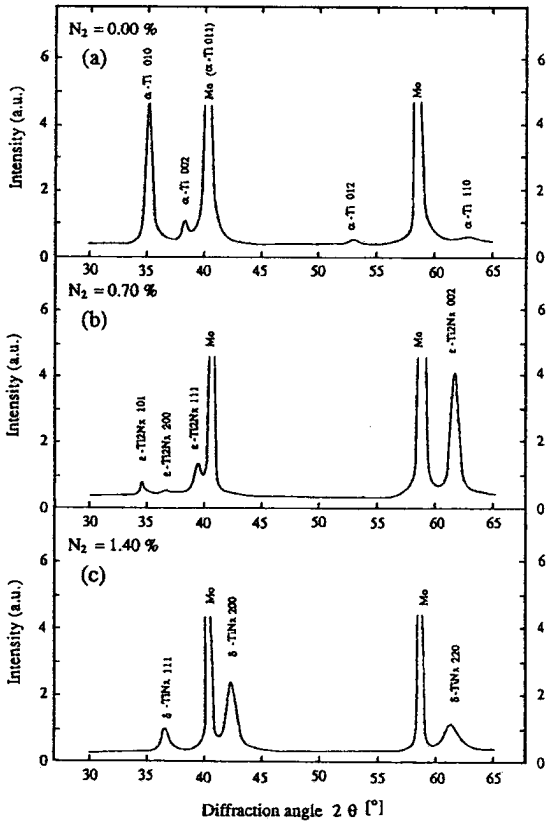

FIG. 5. Selected examples of x-ray diffraction spectra: (a) TiN-1, (b) TiN-3, and (c) TiN-5.

case of TiN_x coatings produced by RIP, that the ϵ-Ti_2N phase occurs only at certain circumstances.[26] According to Ref. 26 the current density should be high enough and the growth rate has to be sufficiently low. Only under these conditions the phases present follow the pattern α-Ti, α-Ti + ϵ-Ti_2N, ϵ-Ti_2N + δ-TiN to single-phase δ-TiN. Lin *et al.* report in the case of TiN_x coatings produced by activated reactive evaporation (ARE) the same pattern.[27]

The preferred orientation of the single-phase δ-TiN coatings was found to be (200) for lower and (220) for higher N_2 concentrations in the process gas. The (111) peak decreases with increasing N_2 concentration and is almost not detectable for higher N_2 concentrations.

3. Microhardness

As a reference the microhardness of an uncoated polished cemented carbide plate has been measured. The determined value was ~1800 HV 0.02.

The value of the measured Vickers hardness of the coatings in dependence of the N_2 concentration in the process gas is shown in Fig. 6. The deviation of the single measured values from the mean value plotted have been smaller than 100 Vickers units. It has been reported, that the measured values depend on load and film thickness.[29,36,37] Usually the determined hardness values are higher at lower loads. It should be mentioned, that the thickness of the coatings investigated is not the same and they are not thick enough to neglect influences of the substrate during measurement at the load used. So the error bars of the measurements can be sometimes higher. As the substrate has a hardness of 1800 HV 0.02, the influence of the substrate on the determined values is almost negligible for similar hardness values, even if the thickness is not sufficient. For low hardness values the indentation depth becomes comparable to the film thickness and the determined values should be to high. For high hardness values the indentation depth decreases and therefore also the influence of the substrate on the determined values at the film thickness in question. These values should have not a high deviation from the true hardness.

As it can be seen in Fig. 6 the hardness at low N_2 concentrations is ~1000 HV 0.02 and increases to ~3000 HV 0.02 with increasing N_2 concentration. At high N_2 concentrations the hardness decreases to ~2000 HV 0.02. One exception of this behavior is in the low N_2 concentration region. The deviation of the measured hardness at 1.05% N_2 from the above-mentioned curve is outside of experimental scattering. The evaluated hardness values are in the range of values which were reported for coatings produced by conventional PVD techniques.[28,29,31,38,39] A comparison of the microhardness of TiN coatings determined by other investigators should be carefully done. Sproul[40] has demonstrated, that he could measure a film hardness of ~3200 kg/mm^2 using an optical microscope and a film hardness of ~2400 kg/mm^2 using a scanning electron microscope. So the conditions under which the measurements were performed has to be taken into consideration. Also the microhardness is strongly influenced by the morphology (grain size and density) and the strain.[41,42] A more detailed discussion will be given later.

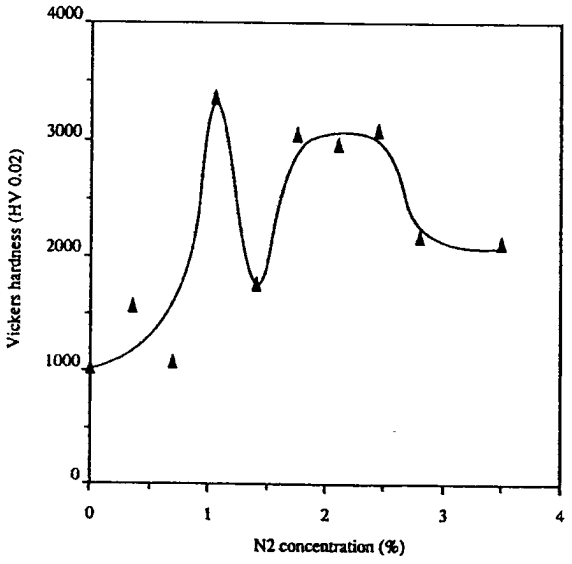

FIG. 6. Effect of N_2 concentration in the process gas on microhardness. Load 20 g.

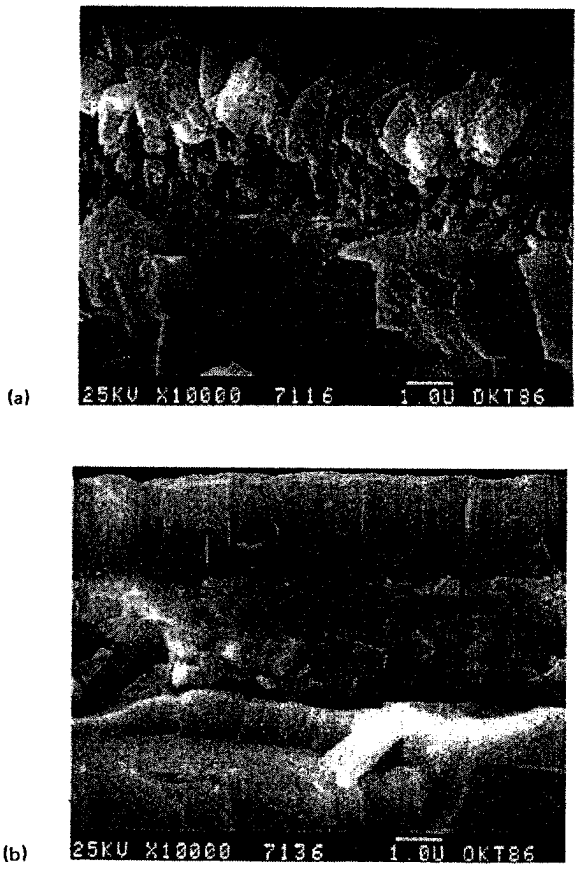

FIG. 7. Scanning electron micrograph showing the typical coating structures (a) TiN-1: single-phase α-Ti and (b) TiN-7: single-phase δ-TiN.

4. Morphology

The TiN_x coatings show a typical dependence of the morphology from the N_2 concentration in the process gas. Figure 7 shows two selected micrographs taken near the fraction plane of a molybdenum substrate coated with (a) single-phase α-Ti and (b) single-phase δ-TiN. The α-Ti phase deposited at zero N_2 concentration shows an open structure with separated crystals and low density. With increasing N_2 concentration the structure changes to densely packed fine granular coatings and finally at high N_2 concentrations ($>1.40\%$) the microstructure becomes a dense columnar morphology. If we compare the observed microstructure with the phases present a correlation can easily be seen. Single-phase α-Ti has an open structure, phase mixtures have a dense fine granular structure, and single-phase δ-TiN has a dense columnar structure. A more detailed study of the morphology would require investigations by transmission electron microscopy (TEM), which was not available.

5. Color

The colors of the deposited TiN_x coatings are given in Table I. The coating at zero N_2 concentration has a grey color. With increasing N_2 concentration the color changes to silver, then to gold, and finally to brown. The colors correspond to the phases present. The single-phase α-Ti is grey, the phase mixtures looks silver and the single-phase δ-TiN shows the gold and brown color.

6. Adhesion

The determined critical load was ~ 35 N for most of the hard coatings deposited. Single values have been much higher (60 N) or lower. Investigations of the indentations by an optical microscope showed purely adhesive failure for low critical loads. This leads to the suggestion, that the critical load is most probably influenced by the interface and therefore by the pretreatment of the substrate. The pretreatment process, especially the transition from sputter cleaning to deposition procedure, was manually controlled and not optimized and should be responsible for the low values and the scattering.

The interface of a coating with poor adhesion (35 N for TiN-8) has been studied by AES. The depth profiling were performed by preparing a crater according to Ref. 37 and 43 with a ball wear scar technique and measure AES spectra along the radius of the crater. No enrichment of impurities in the interface could be observed. In spite of this result, it should be possible to achieve a high and more reproducible adhesion by an optimized and more accurate controlled pretreatment. At the moment the determined adhesion cannot be related to the N_2 concentration in the process gas.

7. Deposition rate

The deposition rate has been determined from the scanning electron micrographs of the fraction planes of the coated molybdenum substrates. The results are shown in Fig. 8. It can be seen, that the rate at zero N_2 concentration is very high. With increasing N_2 concentration the rate decreases to

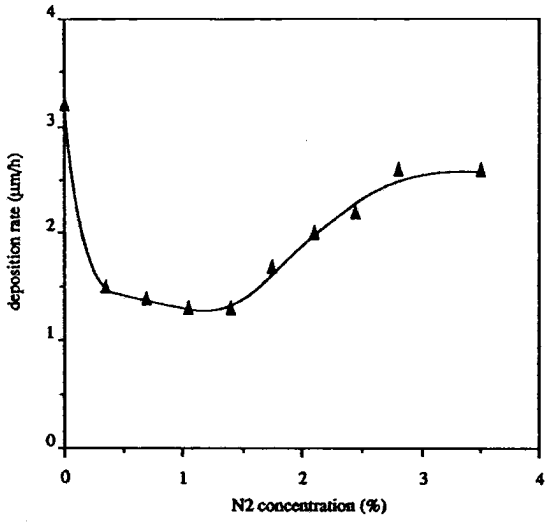

FIG. 8. Effect of N_2 concentration in the process gas on deposition rate.

a constant value of $\sim 1.5\,\mu$m/h, after 1.4% N_2 concentration the rate increases linearly and finally reaches at high N_2 concentrations a constant value of $\sim 2.5\,\mu$m/h. The comparison with the morphology of the coatings shows, that the high rate at zero N_2 concentration corresponds very well with the open structure of low density. The coatings of phase mixtures show a very low rate, but with the apearance of the δ-TiN phase the rate increases steeply. This increase is too steep to be explained by incorporation of N in the coating. This suggests, that higher nitrogen concentration in the process gas has a positive influence on the deposition of titanium.

B. Effect of some other process parameters

This chapter will be restricted to some short remarks, as this subject is in progress and will be extensively described elsewhere.[44]

The effect of the $N_2/TiCl_4$ ratio at constant $TiCl_4$ concentration in the process gas on the deposited coatings has been already described in Sec. III A. In the case of constant high N_2 concentration in the process gas the following behavior can be observed. With increasing $TiCl_4$ concentration the deposition rate increases linearly. This behavior was also observed by Shizhi *et al.* in the case of PACVD in a dc plasma.[9] At higher $TiCl_4$ concentrations the increasing of the deposition rate levels off (it can be compared with the decreasing of the deposition rate with decreasing of N_2 concentration at constant $TiCl_4$ concentration in Fig. 7). Also the chlorine content in the coating is increasing linearly with the increase of the $TiCl_4$ concentration in the process gas. For PACVD in a dc plasma Kikuchi *et al.* have reported a similar dependence (chlorine content versus flow rate of $TiCl_4$).[7]

The dependence of the H_2/Ar ratio on the quality of the deposited coatings shows, that below 50% H_2 in the process gas the properties of the coatings are insufficient, but above 50% H_2 a good quality of the coatings could be achieved. The preferred orientation of δ-TiN at low H_2 concentrations

is in (111), at medium H_2 concentrations in (220) and at high H_2 concentrations in (200). Above 50% H_2 no influence of the H_2/Ar ratio on the chemical composition could be observed.

The rf power has mainly an influence on the deposition rate and chemical composition. With increasing rf power the deposition rate increases and the chlorine content in the coating decreases. Also the preferred orientation changes from (111) to (200).

The self-bias dc voltage on the substrate is influenced by the rf power, pressure, and H_2/Ar ratio in the process gas. With increasing rf power or H_2 concentration the self-bias dc voltage increases and with increasing pressure the self-bias dc voltage decreases. As the self-bias dc voltage cannot be regulated independent of other parameters, the influence of the substrate voltage on the morphology and the mechanical properties of the films cannot be separated without ambiguity. On the other hand additionally to the effect of rf power, pressure, and H_2 concentration, there is a superimposed effect of the substrate voltage.

IV. DISCUSSION

It is seen, that mainly the $TiCl_4$ concentration in the process gas and the rf power influence the deposition rate. With increasing $TiCl_4$ concentration or rf power the deposition rate increases. This behavior is in good agreement with the results reported by Shizhi *et al.*[9] Additionally the N_2 concentration in the process gas shows also an influence on the deposition rate. Higher N_2 concentration seems to have a positive influence on the deposition of titanium.

The composition of the coating can be influenced mainly by the N_2 concentration in the process gas at constant $TiCl_4$ concentration or vice versa. In the case of variable N_2 concentration in the process gas the nitrogen content of the coating increases when the N_2 concentration is increased. Mayr *et al.* have reported a similar behavior.[10] The chlorine content of the coating decreases drastically in presence of N_2 in the process gas. This suggests, that nitrogen or nitrogen compounds play a role in the decomposition of $TiCl_4$ and its subchlorides in the gas phase.

As expected, the phases present are depending on the composition of the coating. At constant $TiCl_4$ flow the phases present follow the pattern α-Ti, α-Ti + ϵ-Ti_2N, predominant ϵ-Ti_2N, ϵ-Ti_2N + δ-TiN to single-phase δ-TiN with increasing N_2 flow and therefore increasing N/Ti atomic ratio. Because of preferential sputtering during the measurement of the composition by AES and the resulting uncertainty in composition it cannot be decided without ambiguity, whether α-Ti or ϵ-Ti_2N still occur at even higher N/Ti atomic ratios as it would be allowed by the bulk phase diagram (Fig. 4).

Coatings consisting of single-phase α-Ti (TiN-1), phase mixtures of α-Ti and ϵ-Ti_2N (TiN-2), or predominant ϵ-Ti_2N phase (TiN-3) exhibit a low hardness. This result is consistent with previously reported results for reactively sputtered films.[3,45]

The highest hardness of all coatings investigated had sample TiN-4, which exhibits a phase mixture of ϵ-Ti_2N + δ-TiN, whereas single-phase δ-TiN showed a lower hardness (TiN-5 to TiN-10). For coatings produced by conventional PVD techniques very high hardness for such phase mixtures have been reported,[27,29,31] but also a low hardness.[3,29] Gabriel *et al.*[31] could achieve a hardness of up to 3150 HV 0.015 for a ϵ-Ti_2N + δ-TiN phase mixture, which was also higher as the highest hardness of δ-TiN in their investigation, and almost equal to the hardness obtained in our investigation (3300 HV 0.02) for such a phase mixture. Lin *et al.*[27] have also reported, that the ϵ-Ti_2N + δ-TiN phase mixture have a higher hardness (Knoop hardness of 2900 HK 0.05) than the single-phase δ-TiN. Sample TiN-4 showed also a fine-grained structure, which is frequently reported for such phase mixtures.[28,30,31,45,46] Investigations by transmission electron microscopy on reactively sputtered Ti–N films showed that δ-TiN has a much smaller grain size in the presence of ϵ-Ti_2N than it does in the absence of this second phase.[28,30] Therefore the higher hardness of the phase mixture might be due to the fine grain size of δ-TiN in the presence of ϵ-Ti_2N. This is consistent with the results presented by Rickerby *et al.*,[41] who observed an increase in hardness by refinement of grain size for single-phase δ-TiN.

Samples TiN-5 to TiN-10, which consist of single-phase δ-TiN, exhibit a columnar structure. The coatings with nearly stoichiometric composition showed the highest hardness of δ-TiN (3000 HV 0.02), whereas with increasing or decreasing nitrogen content the hardness decreases. A similar dependence has been already reported for reactively sputtered δ-TiN,[3,45] but they achieved only a highest hardness of 2300 HV 0.01. Hardness values of stoichiometric δ-TiN, which are close to our determined values or even higher, have been also reported.[28,29,31,38,39,42,47] The large scattering of the published hardness values of stoichiometric δ-TiN is most probably due to different grain size and strain of the coatings.[41,42] The x-ray diffraction peaks of the samples TiN-5 to TiN-10 were relatively broad, which indicates usually either small grain size or large strain.[41,42] The thickness of the coatings of the samples under consideration is in the range of 1.5 to 3.0 μm. Richerby *et al.*[41] have reported, that the hardness of thick coatings is usually lower than that of thin coatings, because of an increase in grain size and porosity towards the surface. In spite of the fact, that in the present work no measurements of strain and grain size have been performed, the observed properties agree with the above-mentioned behavior.

In the present investigation, the residual chlorine content in the coating was minimized to $\sim$1 at. %. Therefore not enough data are available to determine the influence of the chlorine content on the microhardness. Recently Arai *et al.*[12] have reported for TiN films deposited by PACVD in a dc plasma, that they have obtained a hardness comparable to ion-plated TiN coatings for coatings with a chlorine content $<$ 5 wt %. But the hardness decreases continuously with increase in chlorine content. According to these results, the influence of the residual chlorine content of our Ti–N coatings on the microhardness seems to be negligible.

As only for δ-TiN enough measurements of the preferred orientation are available, the discussion of the texture will be restricted to this phase. The preferred orientation changes with the deposition parameters and therefore with the

growth condition. Orientations in (111), (200), and (220) could be observed, as for coatings deposited by conventional PVD techniques.[28] The most significant change in the preferred orientation is from (111) to (200) with increasing H_2 concentration in the process gas or increasing rf power and therefore with increasing self-bias dc voltage. It should be mentioned, that the self-bias dc voltage is only a part of the effective sheath voltage, because of the sometimes very high plasma potential in rf plasmas. In ion plating such a change in the preferred orientation is usually observed with increasing ion current density.[31]

V. SUMMARY AND CONCLUSIONS

The described new plasma reactor is able to produce TiN coatings of high quality at moderate temperature on all surfaces of objects of complex geometry. The quality of this coating is equivalent to the quality obtained by classical CVD and PVD techniques. In the case of δ-TiN phases deposition rates up to 3 μm/h at very low chlorine content in the coating (<1 at. %) could be achieved. In the slightly substoichiometric range of composition, these coatings show the typical golden color, a dense morphology, and a Vickers hardness up to 3000 HV 0.02. So it can be concluded, that the described process is a real alternative to the conventional PVD processes for the deposition of titanium nitride at moderate temperature. The great advantage compared to the conventional methods is, that no movements of the samples are necessary.

ACKNOWLEDGMENT

We thank the Forschungsförderungsfonds für die gewerbliche Wirtschaft for the financial support of this work.

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EXHIBIT L

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC.,	)	
	)	
Plaintiff,	)	
	)	C.A. No. 06-788-JJF
v.	)	
	)	
FREESCALE SEMICONDUCTOR, INC.,	)	
	)	
Defendant.	)	

PLAINTIFF PROMOS TECHNOLOGIES, INC.'S OBJECTIONS AND RESPONSES TO DEFENDANT FREESCALE SEMICONDUCTOR, INC.'S FIRST SET OF REQUESTS FOR ADMISSION (Nos. 1-6)

Pursuant to Rules 26 and 36 of the Federal Rules of Civil Procedure, Plaintiff ProMOS Technologies, Inc. ("ProMOS") hereby submits the following objections and responses to Defendant Freescale Semiconductor, Inc.'s First Set of Requests for Admission (the "Requests").

GENERAL STATEMENT AND OBJECTIONS

ProMOS hereby incorporates by reference its General Statement and Objections from its Objections and Responses to Defendant Freescale Semiconductor, Inc.'s First Set for Production of Requests for Production of Documents and Things as though fully set forth herein.

RESPONSES AND SPECIFIC OBJECTIONS TO REQUESTS

ProMOS also expressly incorporates by reference its General Statement and Objections from its Objections and Responses to Defendant Freescale Semiconductor, Inc.'s First Set for Production of Requests for Production of Documents and Things in response to each of the following Requests and, to the extent they are not raised in any particular response, ProMOS does

not waive those objections. In addition to the objections asserted therein, ProMOS responds as follows:

REQUEST NO. 1:

Admit that the '267 Patent only covers fabrication methods that include the step of forming the claimed titanium nitride layer by physical vapor deposition.

RESPONSE TO REQUEST NO. 1:

ProMOS objects to this request on the ground that it is premature and vague and ambiguous because the claims of the '267 patent have not yet been construed by the Court and Freescale has not defined the term "physical vapor deposition." ProMOS also objects to this interrogatory on the ground that it is premature because it seeks expert opinion. ProMOS will disclose expert opinions at the time and in the manner contemplated by the Scheduling Order entered in this case.

Subject to and without waiving the foregoing general and specific objections, ProMOS states that it can neither admit nor deny this request at this time.

REQUEST NO. 2:

Admit that the '267 Patent does not cover fabrication methods that form the claimed titanium nitride layer by chemical (and not physical) vapor deposition.

RESPONSE TO REQUEST NO. 2:

ProMOS objects to this request on the ground that it is premature and vague and ambiguous because the claims of the '267 patent have not yet been construed by the Court and Freescale has not defined the terms "chemical vapor deposition" or "physical vapor deposition." ProMOS also objects to this interrogatory on the ground that it is premature because it seeks expert opinion. ProMOS will disclose expert opinions at the time and in the manner contemplated by the Scheduling Order entered in this case.

Subject to and without waiving the foregoing general and specific objections, ProMOS states that it can neither admit nor deny this request at this time.

REQUEST NO. 3:

Admit that coverage by the '267 Patent of any fabrication methods that form the claimed titanium nitride layer by chemical (and not physical) vapor deposition was disclaimed during the prosecution of the application leading to the '267 Patent.

RESPONSE TO REQUEST NO. 3:

ProMOS objects to this request on the ground that it is premature and vague and ambiguous because the claims of the '267 patent have not yet been construed by the Court and Freescale has not defined the terms "chemical vapor deposition" or "physical vapor deposition." ProMOS also objects to this request on the ground that it purports to seek a legal conclusion

Subject to and without waiving the foregoing general and specific objections, ProMOS denies this request for admission.

REQUEST NO. 4:

Admit that the '709 Patent has never been licensed to any third party.

RESPONSE TO REQUEST NO. 4:

ProMOS objects to this request on the ground that the term "third party" is vague and ambiguous. ProMOS also objects to this request to the extent that it purports to seek admissions relating to information that is not within ProMOS's possession, custody or control.

Subject to and without waiving the foregoing general and specific objections, ProMOS denies this request for admission.

REQUEST NO. 5:

Admit that the '241 Patent has never been licensed to any third party.

RESPONSE TO REQUEST NO. 5:

ProMOS objects to this request on the ground that the term "third party" is vague and ambiguous. ProMOS also objects to this request to the extent that it purports to seek admissions relating to information that is not within ProMOS's possession, custody or control.

Subject to and without waiving the foregoing general and specific objections, ProMOS denies this request for admission.

REQUEST NO. 6:

Admit that the '267 Patent has never been licensed to any third party.

RESPONSE TO REQUEST NO. 6:

ProMOS objects to this request on the ground that the term "third party" is vague and ambiguous. ProMOS also objects to this request to the extent that it purports to seek admissions relating to information that is not within ProMOS's possession, custody or control.

Subject to and without waiving the foregoing general and specific objections, ProMOS denies this request for admission.

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Dated: July 25, 2007
182592.1

CERTIFICATE OF SERVICE

I hereby certify that on the 25th day of July, 2007, the attached **PLAINTIFF PROMOS TECHNOLOGIES, INC.'S OBJECTIONS AND RESPONSES TO DEFENDANT FREESCALE SEMICONDUCTOR, INC.'S FIRST SET OF REQUESTS FOR ADMISSION (Nos. 1-6)** was served upon the below-named counsel of record at the address and in the manner indicated:

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IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC.,	)	
	)	
Plaintiff,	)	C.A. No. 06-788-JJF
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Dated: July 25, 2007
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CERTIFICATE OF SERVICE

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Discovery Documents

1:06-cv-00788-JJF Promos Technologies Inc. v. Freescale Semiconductor Inc.
PATENT, PaperDocuments

U.S. District Court

District of Delaware

Notice of Electronic Filing

The following transaction was entered by Maguire, Lauren on 7/25/2007 at 3:13 PM EDT and filed on 7/25/2007

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Document Number: 39

Docket Text:
NOTICE OF SERVICE of Objections and Responses to Defendant Freescale Semiconductor, Inc.'s First Set of Requests for Admission (Nos. 1-6) by Promos Technologies Inc..(Maguire, Lauren)

1:06-cv-788 Notice has been electronically mailed to:

Steven J. Balick sbalick@ashby-geddes.com, dfioravanti@ashby-geddes.com, jday@ashby-geddes.com, lmaguire@ashby-geddes.com, mkipp@ashby-geddes.com, nlopez@ashby-geddes.com, rgamory@ashby-geddes.com, tlydon@ashby-geddes.com

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1:06-cv-788 Notice has been delivered by other means to:

The following document(s) are associated with this transaction:

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EXHIBIT M

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